

Making Batteries Last Longer with Fast, High-Precision SAR Analog-to-Digital Converters

By Shane O'Meara

Low power consumption is a key requirement for today's battery-powered analog-to-digital converter applications, as portable handheld instruments for the medical, consumer, and industrial markets trend towards reduced size and weight, longer operating time per battery (or per battery charge), and lower cost, often accompanied by an increased feature set. The benefits of low power, even in non-battery-powered applications, should not be overlooked because low power systems can operate without heat sinks or fans, making them smaller, lower cost, more reliable—and “greener.” In addition, many designers are faced with the challenge of designing products with enhanced features or performance while reducing, or at least not exceeding, existing power budgets.

The huge selection of ADCs on the market today makes choosing the best part to meet specific system requirements ever more challenging. Besides evaluating common converter performance characteristics, such as speed and accuracy, even more specifications need to be considered if low power is a must. Understanding these specifications and how design decisions affect the power budget is essential for determining system power consumption and battery life calculations.

The average power consumption for an ADC is a function of the power used during conversion, the power used while not converting, and the amount of time spent in each mode. This can be expressed by Equation 1.

$$P_{AVG} = (P_{CONV} \times \frac{t_{CONV}}{t_{CONV} + t_{STBY}}) + (P_{STBY} \times \frac{t_{STBY}}{t_{CONV} + t_{STBY}}) \quad (1)$$

P_{AVG} = average power dissipated.

P_{CONV} = power dissipated during conversion.

P_{STBY} = power dissipated during standby or shutdown mode.

t_{CONV} = time spent converting.

t_{STBY} = time spent in standby or power-down mode.

The power used during conversion is usually much greater than the standby power, so the average power can be greatly reduced if the time in standby mode is increased. Successive-approximation (SAR) converter types are particularly amenable to such modes of operation.

One of the biggest factors affecting system power usage is the choice of on-board power supplies. For portable applications, the system will often be powered directly by a 3-V lithium coin cell. This avoids the need for a low dropout voltage regulator, thus saving on power, space, and cost. Nonbattery applications also benefit from converters that have low V_{DD} supply ranges, as power consumption scales with input voltage. Choosing the lowest acceptable V_{DD} for the ADC will result in lower power consumption.

All ADCs that are targeted at low power applications have power-down or standby modes to conserve energy during periods of inactivity. The ADC can be powered down between single conversions, or a burst of conversions can be performed at a high throughput rate, with the ADC powered down between these bursts. For single-channel converters, control of the operating modes can be integrated into the communication interface or can occur automatically once a conversion is complete.

The advantage of integrating the mode control into the communication interface is a reduced pin count. This results in lower power consumption, as there are fewer inputs to drive and less leakage current. Smaller pin counts also lead to smaller package sizes and less I/O required by the MCU. Whatever the control method, careful use of these modes will provide considerable power savings.

Power is reduced in power-down modes, as the name suggests, by turning off parts of the ADC's circuitry. The time required for the circuitry that was shut down to restart conversion determines the throughput rate at which such modes can be used effectively. For an ADC with an internal reference, the restart time will be determined by the time taken to recharge the reference capacitor. Analog-to-digital converters using an external reference require enough time to track the analog input correctly on restart.

For all ADCs on the market today, power scales with throughput. The power consumed is a combination of static and dynamic power. Static power is constant, while the dynamic power scales linearly with throughput. Power savings will, therefore, be made by choosing the lowest possible throughput rate to suit the application.

Figure 1 shows the typical power consumption for the [AD7091R](#), the most recent ultralow power ADC from Analog Devices, as a function of throughput rate. It also shows a comparison of how utilizing the device's power-down mode can provide additional power savings, especially with lower throughput rates. The throughput rate and utilization of the power-down mode of the AD7091R is determined by the device restart time and, as the AD7091R has an on-chip reference, the reference capacitor recharge time. The time it takes to recharge the reference capacitor depends on the capacitance and the level of charge remaining on the capacitor when the on-chip reference restarts.

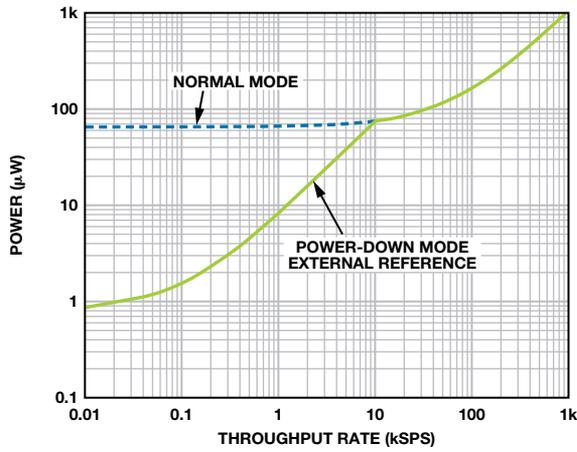


Figure 1. Power vs. throughput for the AD7091R ADC.

The most common methods to initiate conversion requests in ADCs are a dedicated conversion input pin or control via the serial interface. With a dedicated input pin ($\overline{\text{CONVST}}$), a conversion is initiated by a falling edge. The conversion is then controlled by an on-chip oscillator, and the result can be read back via the serial interface once the conversion is complete. Therefore, the conversion is always run at a constant optimum speed, allowing the device to enter low power mode the moment a conversion is complete, thus saving power.

With ADCs where the sampling instant is initiated by a falling edge on chip select ($\overline{\text{CS}}$), the conversion is controlled by the internal sampling clock (SCLK) signal. The SCLK frequency will affect the conversion time and the achievable throughput rate—and, therefore, the power consumption. The faster the SCLK rate, the shorter the conversion time. With shorter conversion time, the proportion of time available for the device to be in low power mode increases compared to normal mode; therefore, significant power savings can be achieved. That is, if each conversion requires N cycles of the SCLK, then for S conversions per second, the total time the SCLK is switching is $S \times N/f_{\text{SCLK}}$, and the quiescent time per second is shown in Equation 2.

$$\left(1.00 - \frac{S \times N}{f_{\text{SCLK}}}\right) \quad (2)$$

Thus, for a given number of samples per second, as f_{SCLK} increases, the quiescent time per second also increases.

For example, assuming 16 SCLK cycles to complete a conversion and read the results, a system sampling at 100 kSPS with a 30 MHz SCLK will be quiescent 94.67% of the time, that is, it will spend 5.33% of the time converting (53.3 ms per second). The same system operating with a 10-MHz SCLK will be quiescent only 84% of the time, that is, it will spend 160 ms converting. Therefore, to achieve the optimum power consumption, the converter should be operated at the highest allowable SCLK frequency.

An important but frequently overlooked parameter when designing for low power is the capacitive load seen at the output pins, especially the communication interface pins, such as SCLK, $\overline{\text{CS}}$, and SDO, as these I/O variables are constantly changing state during the conversion process. The capacitive load seen at an output is the pin capacitance of the driver IC itself, plus the pin capacitance of the input pin, plus the PCB trace capacitance. The trace capacitance can generally be kept small, in the femtofarad range, and is not significant. The power required to charge a capacitive load (P_L) is a function of the load (C_L), the drive voltage (V_{DRIVE}), and the frequency of change (f), as defined by Equation 3.

$$P_L = C_L \times V_{\text{DRIVE}}^2 \times f \quad (3)$$

The power for a complete system is, therefore, the sum of the products of the load capacitance (C_{Ln}) times the switching frequency (f_n) multiplied by the square of the drive voltage.

$$P_L = \sum (C_{Ln} \times f_n) \times V_{\text{DRIVE}}^2 \quad (4)$$

As the ADC drives the SDO pin, and the host microcontroller drives the $\overline{\text{CS}}$, $\overline{\text{CONVST}}$, and SCLK pins, the lowest power consumption will be achieved by minimizing pin capacitance for all devices.

For the $\overline{\text{CS}}$ and $\overline{\text{CONVST}}$ pins, the switching frequency is determined solely by the throughput rate. The SCLK frequency, as already discussed, should be set to the maximum allowable frequency to reduce power. This is not a contradiction: the important point is that the SCLK is not free running—it should be active for only the minimum possible time to propagate the result on the SDO line for each bit trial and to control the conversion process. This is device- and resolution dependent but is typically one cycle per bit, plus some overhead, or about 16 SCLK cycles per sample for 12-bit converter SPI interfaces. The minimum frequency for the SCLK is, therefore, the number of cycles required multiplied by the throughput rate.

The frequency of the SDO line depends on both the throughput rate and the conversion result. While this is not controllable, designers should understand how it can affect power consumption for a conversion. The highest power consumption will occur when the result is a 101010... sequence; the lowest will occur when the result is all 1s or all 0s.

Besides lower throughput rate, decreased V_{DRIVE} voltage will also reduce power consumption considerably. Analog-to-digital converters have either a single-supply pin or separate supplies for the analog circuitry and digital interface. A separate V_{DRIVE} supply gives more design flexibility and avoids the need for level shifters, as the analog-to-digital interface voltage can be matched to that of the SPI master. Choosing the lowest voltage available for V_{DRIVE} will correspond to the lowest system power consumption.

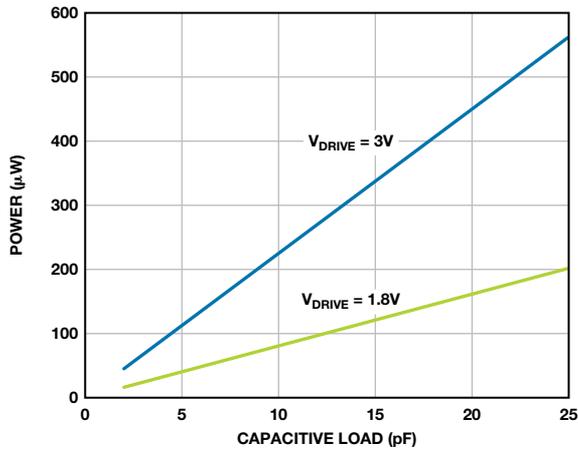


Figure 2. Typical interface power consumption vs. capacitive load.

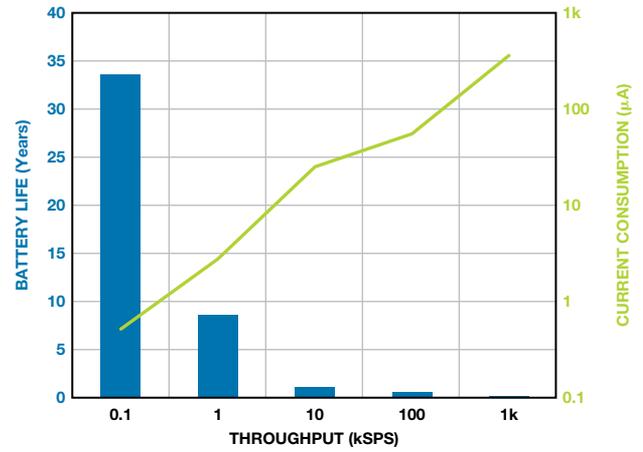


Figure 3. Battery life and current consumption vs. throughput for the AD7091R.

Figure 2 compares the typical power requirement of a standard SPI interface—with CS, SDO, and SCLK—as a function of total capacitive load for V_{DRIVE} values of 3 V and 1.8 V, throughput rate of 100 kSPS, 16 SCLK cycles per conversion, and a worst case SDO output of 1010... for a 12-bit ADC.

Other typical constituents of an ADC circuit design are a voltage reference and an operational amplifier. It goes without saying that these components should also be chosen carefully for low power. Some references are available with power-down modes to reduce consumption during periods of inactivity. The choice of amplifier is application dependent, so the system throughput rate should be considered to ensure that the chosen amplifier maximizes the ADC performance and minimizes power consumption.

The 12-bit AD7091R, specifically designed for low power applications, features an SPI interface, an on-chip precision 2.5-V voltage reference, and a 1-MSPS sampling rate. Conversions are initiated via a $\overline{\text{CONVST}}$ pin. An on-chip oscillator controls the conversion process, making it possible to optimize power consumption. The pin capacitance is a low 5 pF maximum. A wide input voltage range (2.7 V to 5.25 V) allows for integration into a wider range of applications than just battery-powered ones. A separate V_{DRIVE} supply of 1.65 V to 5.25 V allows for reduced power and greater system integration capabilities.

When operating at 1 MSPS, the AD7091R draws 349 μA typical at 3-V V_{DD} . Since its power scales with throughput, 55- μA quiescent current is achievable at 100 kSPS. Static current when not converting, but with the reference active, is 21.6 μA ; in power-down mode, only 264 nA is drawn. The AD7091R is available in 10-lead MSOP or LFCSP packages.

Typical amplifiers to drive the AD7091R would include the AD8031—for fast throughput applications—and the AD8420 for lower bandwidth applications. The quiescent current consumption of the AD8031 is 750 μA typical with a 2.7-V supply; that of the AD8420 is 70 μA typical when used with a 5-V supply.

Figure 3 shows typical current consumption and calculated battery life for the AD7091R when supplied via a CR2032 lithium battery. It can be clearly seen that as throughput decreases, battery life can be greatly extended.

When the AD7091R is compared to most other ADCs, significant savings can be achieved in the power budget. For example, when matched against the nearest available competition, a part with no internal reference, for a 1-MSPS throughput rate, the AD7091R achieves better than a 3 \times reduction in power consumption (1 mW typical compared to 3.9 mW typical for a 3-V supply). This corresponds to extending the battery life of a CR2032 battery by 400 hours. When the other device's need for an external voltage reference is taken into account, the savings are further increased.

Conclusion

There are many benefits of reduced power consumption other than increased battery life. Less heat is generated, which leads to smaller form factors. Reliability improves due to the lower temperature stress. System costs can be lowered, as PCB size can be reduced due to the smaller components—with a reduction in number of components, as there is no need for such accessories as heat sinks.

This article has outlined several important considerations and advantages that the system designer should take into account regarding optimization of power consumption in their designs employing ADCs.

References

Casamayor, Mercedes and Claire Croke. "How to Save Power in Battery Applications Using the Power-Down Mode in an ADC." *Analog Dialogue*, Vol. 37, No. 3, pp. 3-9, 2003.

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