

# How to Apply Low-Dropout Regulators Successfully

By Ken Marasco

A low-dropout regulator (LDO) is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to a very small difference between input and output voltages. This difference, known as the dropout voltage or headroom requirement, can be as low as 80 mV at 2 A. The adjustable-output low-dropout regulator<sup>1</sup> first came to public attention in 1977. Nowadays, portable devices often require up to 20 low-dropout linear regulators. Many of the LDOs in today's portable devices are integrated into multifunction [power-management ICs](#)<sup>2</sup> (PMICs)—highly integrated systems with 20 or more power domains for audio, battery charging, housekeeping, lighting, communications, and other functions.

As portable systems rapidly evolve, however, the integrated PMIC cannot keep up with peripheral power requirements. Dedicated LDOs must be added in the later stages of system development to power such optional items as camera modules, Bluetooth, WiFi, and other bolt-on modules. LDOs have also been used as band-aids for noise reduction, to solve voltage-regulation problems caused by electromagnetic interference (EMI) and printed-circuit board (PCB) routing, and to improve system efficiency by switching off unneeded functions.

This article reviews the basic LDO topology, explains key specifications, and shows the application of low-dropout voltage regulators in systems. Examples will be given using design characteristics of [Analog Devices LDO families](#).<sup>3</sup>

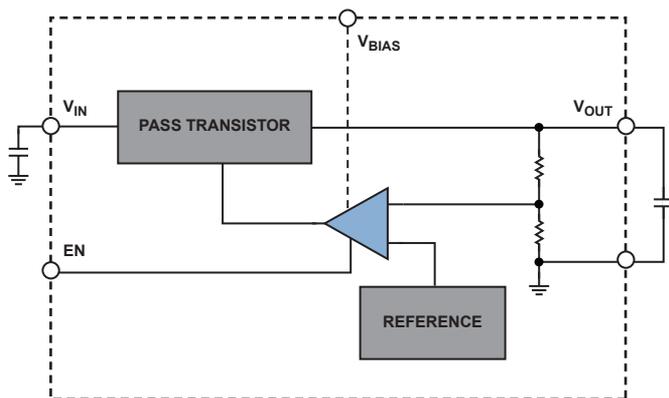


Figure 1. An LDO regulates the output voltage with a low dropout voltage (the difference between  $V_{OUT}$  and the lowest specified value of  $V_{IN}$  at the rated load current).

**Basic LDO Architecture.**<sup>4</sup> An LDO consists of a voltage reference, an error amplifier, a feedback voltage divider, and a pass transistor, as shown in Figure 1. Output current is delivered via the pass device. Its gate voltage is controlled by the error amplifier—which compares the reference voltage with the feedback voltage, amplifying the difference so as to reduce the error voltage. If the feedback voltage is lower than the reference voltage, the gate of the pass transistor is pulled lower, allowing more current to pass and

increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the pass transistor is pulled higher, restricting the current flow and decreasing the output voltage.

The dynamics of this closed-loop system are based on two main poles—the internal pole formed by the error amplifier/pass transistor and the external pole formed by the amplifier's output impedance and the output capacitor's equivalent series resistance (ESR). The output capacitance and its ESR affect the loop stability and the response to transient changes in load current. An ESR of 1  $\Omega$  or less is recommended to ensure stability. Also, LDOs require input and output capacitors to filter noise and control load transients. Larger values improve the transient response of the LDO but increase the startup time. Analog Devices LDOs are designed to be stable over the specified operating conditions when the specified capacitors are used.

**LDO Efficiency.** Increased efficiency is a constant demand from the design engineer. This translates into a reduction of the quiescent current ( $I_Q$ ) and forward voltage drop.

$$\text{LDO efficiency} = \left( \frac{V_{OUT} \times I_{OUT}}{V_{IN} (I_{OUT} + I_Q)} \right) \times 100\% \quad (1)$$

With  $I_Q$  in the denominator, it is evident that the higher  $I_Q$ , the lower the efficiency. Today's LDOs have reasonably low  $I_Q$ , and for simplicity,  $I_Q$  can be neglected in efficiency calculations if  $I_Q$  is very small compared to the load current,  $I_{OUT}$ . Then LDO efficiency is simply  $(V_{OUT}/V_{IN}) \times 100\%$ . Because the LDO has no way to store significant amounts of unused energy, power not delivered to the load is dissipated as heat within the LDO.

$$\text{Power dissipated } (P_D) = (V_{IN} - V_{OUT}) \times I_{IN} \quad (2)$$

Providing a stable power supply voltage independent of load and line variations, changes in ambient temperature, and the passage of time, LDOs are most efficient with small differences between supply voltage and load voltage. For example, as a lithium-ion battery drops from 4.2 V (fully charged) to 3.0 V (discharged), a 2.8-V LDO connected to the battery will maintain a constant 2.8 V at the load (dropout voltage less than 200 mV), but its efficiency would increase from 67% with the fully charged battery to 93% with the discharged battery.

To improve efficiency, LDOs can be connected to an intermediate voltage rail generated by a high-efficiency switching regulator. With a 3.3-V switching regulator, for example, the LDO efficiency would be constant at 85%, and the overall system efficiency would be 81%, assuming 95% efficiency for the switching regulator.

**Circuit Features Enhance LDO Performance.** An enable input permits external control of LDO turn-on and turn-off, allowing supplies to be sequenced in proper order in multi-rail systems. Soft-start limits inrush current and controls output-voltage rise time during power-up. A sleep state minimizes power drain, especially useful in battery-based systems, while allowing fast turn-on. Thermal shutdown turns the LDO off if its temperature exceeds the specified value. Over-current protection limits the LDO's output current and power dissipation. Under-voltage lockout disables the output when the supply voltage is below the specified minimum value. Figure 2 shows a simplified typical power system for portable designs.

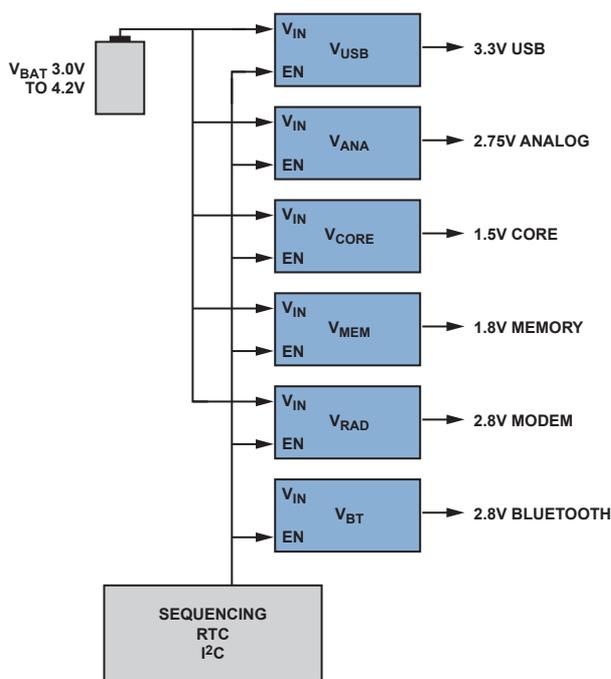


Figure 2. Typical power domains in a portable system.

### Understanding Linear Regulator Requirements

**LDOs for Digital Loads.** Digital linear regulators, such as the [ADP170](#) and [ADP1706](#), are designed to support the main digital requirements of a system, usually microprocessor cores and system input/output (I/O) circuitry. LDOs for DSPs and microcontrollers have to work with good efficiency and handle high and rapidly varying currents. Newer application requirements put tremendous strain on the digital LDO because processor cores often change clock speed to save energy. The clock-speed variation, in response to software-induced loading, translates into a demanding need for LDO load-regulation capability.

The important characteristics for digital loads are line- and load regulation and transient under- and overshoot. When powering low-voltage microprocessor cores, accurate output-control is very important at all times; inadequate regulation can allow the core to latch up. The above parameters are not always featured in data sheets, and graphs of transient response may show optimistic rise and fall speed in response to transient signals. Line and load regulation is stated in two ways: percent deviation of output voltage with load change, actual V/I values, or both, at a specific load current.

To save energy, digital LDOs are designed with low  $I_Q$  to increase battery life, and portable systems have long periods of low-power operation when the software is idling. During periods of inactivity, systems will go to sleep—requiring the LDO to shut down and consume less than  $1\ \mu\text{A}$ . While the LDO is in sleep mode, all of the circuits—including the band-gap reference—are switched off. When the system returns to active mode, fast turn-on times are required—during which the digital supply voltage must not overshoot excessively. Excessive overshoot can result in system latch up, sometimes requiring the removal of the battery or activation of the master reset button to correct the problem and restart the system.

**LDOs for Analog and RF Loads.** Low noise and high power supply rejection (PSR), as found in the [ADP121](#) and [ADP130](#), are important for LDOs used in the analog environment because analog devices are more sensitive to noise than digital devices.

Analog LDO requisites are mainly driven by the wireless interface requirements: “Do no harm to the receiver or transmitter, and create no pop or hum in the audio system.” The wireless connection is highly susceptible to noise, and the receiver’s effectiveness can be reduced if the noise interferes with the signal. When considering an analog linear regulator, it is important for the device to suppress noise from upstream sources and downstream loads, while not adding further noise itself.

Analog regulator noise is measured in volts rms and PSR, its ability to suppress upstream noise. Adding an external filter or a bypass capacitor can reduce noise, but it adds cost and size. Noise reduction and supply-noise rejection can also be achieved by care and ingenuity in the LDO’s internal design. When selecting LDOs, it is important to review the product details in relation to the overall performance needed for each system.

### Key LDO Specifications and Definitions

**Note:** Specifications on the front page of manufacturers’ datasheets are brief summaries, often presented in a way that emphasizes the device’s attractive features. The key parameters often emphasize typical performance characteristics, which can be more fully understood only when consulting the complete specifications and other data within the body of the document. Also, because there is little standardization among manufacturers in the way specifications are presented, power designers need to understand the definition and the methodology used to obtain key parameters listed in the electrical specifications table. The system designer should pay close attention to key parameters, such as ambient and junction temperature range, X-Y scales of graphic information, loads, rise- and fall times of transient signals, and bandwidth. We list here a discussion of important parameters relating to the characterization and application of Analog Devices LDOs.

**Input Voltage Range:** An LDO’s input voltage range determines the lowest usable input supply voltage. The specifications may show a wide input-voltage range, but the lowest input voltage must be greater than the dropout voltage plus the desired output voltage. For example a 150-mV dropout means that the input voltage must be above 2.95 V for a regulated 2.8-V output. If the input voltage drops below 2.95 V, the output voltage will drop below 2.8 V.

**Ground (Quiescent) Current:** The quiescent current,  $I_Q$ , is the difference between the input current,  $I_{IN}$ , and the load current,  $I_{OUT}$ , measured at the specified load current. For fixed-voltage regulators,  $I_Q$  is the same as the ground current,  $I_G$ . For adjustable-voltage regulators, such as the [ADP171](#), the quiescent current is the ground current minus the current from the external resistance-divider network.

**Shutdown Current:** The input current consumed when the device has been disabled. Usually below  $1.0\ \mu\text{A}$  for portable LDOs, this specification is important for battery charge life during long standby times when the portable device is turned off.

**Output Voltage Accuracy:** Analog Devices LDOs are designed for high output-voltage accuracy; they are factory-trimmed to within  $\pm 1\%$  at  $25^\circ\text{C}$ . Output-voltage accuracy is specified over the operating-temperature, input-voltage, and load-current ranges; error is specified as  $\pm x\%$  worst case.

**Line Regulation:** Line regulation is the change in output voltage for a change in the input voltage. To avoid inaccuracy due to changes in chip temperature, the measurement is made under conditions of low power dissipation or by using pulse techniques.

**Dynamic Load Regulation:** Most LDOs can easily hold the output voltage nearly constant as long as the load current changes slowly. When the load current changes quickly, however, the

output voltage will change briefly. How much the output voltage changes when subjected to a change in load current defines load transient performance.

**Dropout Voltage:** Dropout refers to the smallest difference between input and output voltages required to maintain regulation. That is, an LDO can hold the output load voltage constant as the input is decreased until the input reaches the output voltage plus the dropout voltage, at which point the output “drops out” of regulation. The dropout voltage should be as low as possible to minimize power dissipation and maximize efficiency. Typically, dropout is considered to be reached when the output voltage has dropped to 100 mV below its nominal value. The load current and junction temperature can affect the dropout voltage. The maximum dropout voltage should be specified over the full operating temperature range and load current.

**Start-Up Time:** Start-up time is defined as the time between the rising edge of the enable signal and  $V_{OUT}$  reaching 90% of its nominal value. This test is usually performed with  $V_{IN}$  applied and the enable pin toggled from off to on. Note: in some cases where the enable is connected to  $V_{IN}$ , the startup time can substantially increase because the bandgap reference takes time to stabilize. Start-up time of a regulator is an important consideration for applications where the regulator is frequently turned off and on to save power in portable systems.

**Current-Limit Threshold:** Current limit threshold is defined as the load current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0-V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

**Operating Temperature Range:** Operating temperature range can be specified by ambient and junction temperature. Because an LDO dissipates heat, the IC will always operate above the ambient. How much above the ambient temperature depends on the operating conditions and the PCB thermal design. A maximum junction temperature ( $T_J$ ) is specified because operation above the maximum junction temperature for extended periods may affect device reliability—statistically specified as mean time to failure (MTTF).

**Thermal Shutdown (TSD):** Most LDOs have silicon thermostats for protecting the IC from thermal runaway. They are used to power down the LDO if the junction temperature exceeds the specified thermal shutdown threshold. Hysteresis is required to allow the LDO to cool down before restarting. TSD is important because it protects more than the LDO alone; excessive heat affects more than just the regulator. Heat conducted from the LDO to the PCB (or to the LDO from hotter elements on the board) can damage the PCB material and solder connections over time, and also damage nearby components, reducing the life of the portable device. Also, thermal shutdown affects system reliability. Thermal design to control the board temperature (heat sinking, cooling, etc.) is thus an important system consideration.

**Enable Input:** LDO enables, offered in positive and negative logic, turn the device on and off. Active-high logic enables the device when the enable voltage exceeds the logic high threshold. Active-low logic enables the device when the enable voltage is below the logic low threshold. The enable input permits external control of LDO turn-on and turn-off, an important feature in the sequencing of supplies in multi-rail systems. Some LDOs have substantially shorter startup times, because their band-gap reference is on while the LDO is disabled, allowing the LDO to turn on faster.

**Under-Voltage Lockout:** Under-voltage lockout (UVLO) will ensure voltage is supplied to the load only when the system input voltage is above the specified threshold. UVLO is important because it only allows the device to power on when the input voltage is at or above what the device requires for stable operation.

**Output Noise:** The LDO’s internal band-gap voltage reference is the source of noise, usually specified in microvolts rms over a specific bandwidth. For example, the ADP121 has an output noise of 40  $\mu$ V rms from 10 kHz to 100 kHz at a  $V_{OUT}$  of 1.2 V. When comparing datasheet specifications, the specified bandwidth and operating conditions are important considerations.

**Power-Supply Rejection:** PSR, expressed in decibels, is a measure of how well the LDO rejects ripple from the input power supply over a wide frequency range (1 kHz to 100 kHz). In an LDO, PSR can be characterized in two frequency bands. Band 1 is from dc to the control loop’s unity-gain frequency; PSR is set by the open-loop gain of the regulator. Band 2 is above the unity-gain frequency; PSR is unaffected by the feedback loop. Here PSR is set by the output and any leakage paths from the input to the output pins. Choosing a suitably high-value output capacitance will typically improve PSR in this latter band. In Band 1, Analog Devices proprietary circuit design reduces changes in PSR due to input voltage and load variations. For optimum supply rejection, the PCB layout must be considered to reduce the leakage from input to output, and grounding should be robust.

**Minimum Input- and Output Capacitance:** The minimum input- and output capacitance should be greater than specified over the full range of operating conditions, especially operating voltage and temperature. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R- and X5R-type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

**Reverse-Current Protection Feature:** A typical LDO with a PMOS pass device has an intrinsic body diode between  $V_{IN}$  and  $V_{OUT}$ . When  $V_{IN}$  is greater than  $V_{OUT}$ , this diode is reverse-biased. If  $V_{OUT}$  is greater than  $V_{IN}$ , the intrinsic diode becomes forward-biased and conducts current from  $V_{OUT}$  to  $V_{IN}$ , potentially causing destructive power dissipation. Some LDOs, such as the [ADP1740/ADP1741](#), have additional circuitry to protect against reverse current flow from  $V_{OUT}$  to  $V_{IN}$ . The reverse current protection circuitry detects when  $V_{OUT}$  is greater than  $V_{IN}$  and reverses the direction of the intrinsic diode connection, reverse-biasing the diode.

**Soft Start:** Programmable soft start is useful for reducing inrush current upon startup and for providing voltage sequencing. For applications that require a controlled inrush current at startup, LDOs such as the ADP1740/ADP1741 provide a programmable soft-start (SS) function. To implement soft start, a small ceramic capacitor is connected from SS to GND.

## Conclusion

LDOs perform a vital function. Though simple in concept, there are many factors to consider in applying them. This article has reviewed basic LDO topology, and explained key specifications and application of low-dropout voltage regulators in systems. Data sheets contain much helpful information. Further information (selection guides, data sheets, application notes)—as well as ways to get human help—is available on the [power management](#)<sup>5</sup> web site. Also available is [ADIsimPower](#)<sup>TM6</sup>, the fastest, most accurate dc-to-dc power management design tool.

## References

(Information on all ADI components can be found at [www.analog.com](http://www.analog.com))

<sup>1</sup> Dobkin, R., “Break Loose from Fixed IC Regulators,” *Electronic Design*, April 12, 1977.

<sup>2</sup> [www.analog.com/en/power-management/multifunction-power-ics/products/index.html](http://www.analog.com/en/power-management/multifunction-power-ics/products/index.html)

<sup>3</sup> [www.analog.com/en/power-management/linear-regulators/products/index.html](http://www.analog.com/en/power-management/linear-regulators/products/index.html)

<sup>4</sup> Patoux, J., [Low-Dropout Regulators](#) (Ask The Applications Engineer—37), *Analog Dialogue* 41-2 (2007), pp. 8-10. [www.analog.com/library/analogDialogue/archives/41-05/ldo.html](http://www.analog.com/library/analogDialogue/archives/41-05/ldo.html)

<sup>5</sup> [www.analog.com/en/power-management/products/index.html](http://www.analog.com/en/power-management/products/index.html)

<sup>6</sup> <http://designtools.analog.com/dtPowerWeb/dtPowerMain.aspx>

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