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Editor's Notes

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Current feedback amplifiers (CFA) are not typically used as transimpedance amplifiers due to their relatively high inverting input current and current noise. CFAs are easy to use, however, and can outperform their voltage feedback counterparts in applications that require high gain, low power, low noise, wide bandwidth, and high slew rate. This article shows how to properly compensate CFAs. (Page 3)

Amplifier Disable Function Eliminates Need for Multiplexers in Multichannel Applications
A multiplexer routes the signal from one of several inputs to a common output. Many applications use amplifiers to condition the signal before the mux. In these cases, amplifiers with a disable function can be used to select the channel, eliminating the need for a mux—reducing cost, PCB area, and distortion. This article presents the challenges of using op amps with a disable function for channel selection. (Page 7)

Minimizing Errors in Multiplexed 3-Wire RTD Data-Acquisition Systems
In a programmable logic controller or a distributed control system, one data-acquisition module may monitor the temperature of many remotely located resistance temperature detectors (RTDs). The best accuracy will be obtained when each RTD has its own excitation circuit and ADC, but the module will be large, expensive, and power hungry. Multiplexing leads to a smaller, lower cost, lower power module. (Page 9)

System Demonstration Platform Eases Transition from Evaluation to Prototyping
To simplify selecting components for new designs, Analog Devices provides evaluation boards and application software, but the best way to save time and increase the chance of success is to have the code and interface ready before the board is built. The System Demonstration Platform was designed to allow this type of prototyping, making it simpler than ever to kick start system development. (Page 11)

Reduced Integration Time Improves Accuracy in Dead Reckoning Navigation Systems
Automotive dead reckoning navigation systems use gyroscopes to estimate the vehicle's instantaneous heading. Combined with the distance traveled, this allows the navigation system to correctly determine the vehicle's position when the satellite signal is blocked. If the satellite signal is lost for a long time, the accumulated angle error will become large. This article offers a simple way to minimize this problem. (Page 13)

How to Design and Debug a Phase-Locked Loop (PLL) Circuit
Designing and debugging a phase-locked loop (PLL) circuit can be complicated, unless engineers have a deep understanding of PLL theory and a logical development process. Many problems can be avoided by paying close attention during the design phase, so this article presents a simple methodology for PLL design and provides an effective, logical way to debug PLL problems. (Page 15)

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PRODUCT INTRODUCTIONS: VOLUME 47, NUMBER 3

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July

Accelerometer, MEMS, digital, 3-axis, ±0.5-*g*/±1-*g*/±2-*g*/±4-*g* **ADXL313**
PMU, 5-channel, four buck regulators, one LDO **ADP5050/ADP5052**
Synthesizer, frequency, 13-GHz, fractional-N **ADF4159**

August

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Amplifier, variable-gain, 1100-MHz, programmable filter **ADRF6518**
Charger, battery, linear $LiFePO_4$, USB-compatible **ADP5063**
Microphone, MEMS, RF-hardened, ultralow-noise, analog **ADMP510**
Processors, embedded, Blackfin® dual-core **ADSP-BF60x**
Regulator, linear, ultralow-noise, 200-mA **ADM7160**

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Amplifier, operational, CMOS, precision, RRIO **ADA4661-2**
Amplifier, operational, high-temperature, low-power **AD8634**
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Compensating Current Feedback Amplifiers in Photocurrent Applications

By Jonathan Pearson

Introduction

Historically, current feedback amplifiers (CFA) have not been the first choice for use as transimpedance amplifiers (TIA) due to their relatively high inverting input currents and inverting input current noise, which can be at least an order of magnitude larger than that of a comparable voltage feedback amplifier (VFA). Additionally, many system designers are unfamiliar with CFAs, so they're less comfortable using them. The fact remains, however, that CFAs are quite easy to use and can outperform their VFA counterparts in applications that require high gain, low power, low noise, wide bandwidth, and high slew rate. One of their main benefits is that the loop gain of an *ideal* CFA is independent of its closed-loop gain, thus allowing the CFA to deliver excellent harmonic distortion and bandwidth performance irrespective of its closed-loop gain.

Due to their very low input bias current and input current noise, FET-input op amps are often given the highest consideration for TIA applications, particularly those that use low output current devices, such as photoelectric elements, as the input current source. While FET-input amplifiers do excel in many of these applications, their speed can be insufficient in systems that require faster performance. Thus, CFAs are increasingly being used as TIAs in faster systems that can tolerate more noise.

This article deals with how the parasitic capacitance of a photodiode or other light-to-current transducer affects a CFA operating as a TIA, and how to properly compensate the amplifier for this capacitance. Some introductory material regarding CFA operation is provided, as well as occasional parallels between CFA and VFA analyses. Analysis of the "noise gain" of VFA circuits or "feedback impedance" of CFA circuits is not used. Instead, classical feedback theory using loop gain is used to avoid difficulties incurred when moving between current and voltage domains (loop gain is always a dimensionless quantity) and because the theory itself presents Bode plots that are straightforward and easy to use.

Current Feedback Amplifier Basics

An ideal CFA has zero input impedance—a dead short across its inputs—because the negative feedback signal is a current. In contrast, an ideal VFA has infinite input impedance because its feedback signal is a voltage. The CFA senses the error current flowing in its input and develops an output voltage equal to Z times the input current, where Z represents the transimpedance gain. The direction of the error current is defined to produce negative feedback. Similar to A in a VFA, Z approaches infinity in an ideal CFA. Figure 1 shows the basics of how an ideal CFA could be configured as a TIA to transfer the current from an ideal current source to its output voltage.

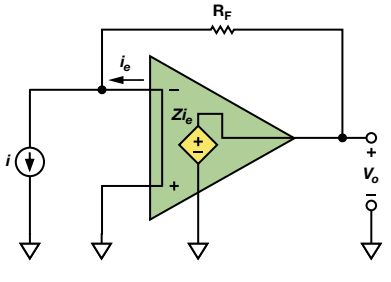

Figure 1. Ideal CFA used as a TIA.

The closed-loop gain of this TIA can be expressed as

$$\frac{v_o}{i} = R_F\left[\frac{1}{1+\frac{R_F}{Z}}\right] \quad (1)$$

Equation 1 shows that as Z approaches infinity, the TIA gain approaches its ideal value of R_F. As Z approaches infinity, the error current, i_e, approaches zero, and all of the input current flows through R_F. The loop gain is seen as $\frac{Z}{R_F}$ in Equation 1.

Unfortunately, ideal CFAs do not exist, so practical devices use the next best thing: a unity-gain buffer across their inputs. A current mirror reflects the error current to a high-impedance node where it is converted to a voltage, buffered, and fed to the output, as shown in Figure 2.

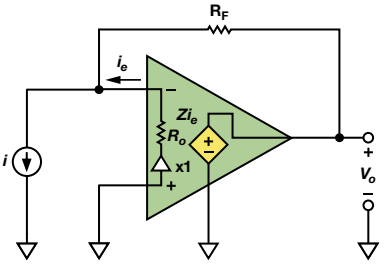

Figure 2. Practical CFA with unity-gain buffer used as a TIA.

As long as $R_o = 0$, the closed-loop gain is the same as that given in Equation 1. When $R_o > 0$, the closed-loop gain becomes

$$\frac{v_o}{i} = R_F\left[\frac{1}{1+\frac{R_F+R_O}{Z}}\right] \quad (2)$$

and the loop gain is $\frac{Z}{R_F+R_O}$.

TIA Design Using Practical Components

Photodiode and other photoelectric devices exhibit a parasitic shunt capacitance proportional to the device area. When $R_o = 0$, this capacitance is fully bootstrapped, so it has no effect on the closed-loop response. In a real CFA, $R_o > 0$, and the parasitic capacitance influences the response, potentially causing the circuit to become unstable. In addition, like the open-loop gain, A, in a VFA, the magnitude of Z in a real CFA is large at low frequency and rolls off with increasing frequency, and the phase shift lags more with increasing frequency. To first order, Z(s) can be characterized with a single dominant pole at $s = p$ and dc transimpedance of Z_O, as shown in Equation 3. High frequency poles in Z(s) will be considered later.

$$Z(s) = \frac{Z_O}{1-\frac{s}{p}} \quad (3)$$

The circuit in Figure 3 includes the parasitic capacitance, C, and the transimpedance, Z(s). Note that the CFA's inverting input capacitance can be absorbed into C.

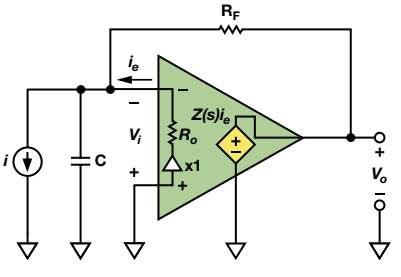

Figure 3. Practical CFA-based TIA including parasitic capacitance.

Equation 4 is derived by performing KCL at the inverting input.

$$\frac{v_o + i_e R_o}{R_F} = -i_e - i_e R_o C s + i \tag{4}$$

The error current, i_e, is

$$i_e = \frac{v_o}{Z(s)} \tag{5}$$

Combining Equation 4 and Equation 5 produces the following result for the closed-loop TIA gain of the circuit in Figure 3:

$$\frac{v_o}{i} = R_F \left[\frac{1}{1 + \dfrac{R_F R_o C \left(s + \dfrac{1}{(R_F \| R_o) C} \right)}{Z(s)}} \right] \tag{6}$$

The loop gain is evident in Equation 6 and is given by

$$\text{Loop Gain} = \frac{Z(s)}{R_F R_o C \left(s + \dfrac{1}{(R_F \| R_o) C} \right)} = \left[\frac{Z_O}{1 - \dfrac{s}{p}} \right] \left[\frac{1}{R_F R_o C \left(s + \dfrac{1}{(R_F \| R_o) C} \right)} \right] \tag{7}$$

The loop gain contains two poles, a low-frequency pole at $s = p$ and a high-frequency pole at $s = -\dfrac{1}{(R_F \| R_o) C}$. When $R_o << R_F$, the parallel combination of R_F and R_o can be approximated by R_o. The two poles present a stability problem when the high-frequency pole occurs at a frequency where the magnitude of the loop gain is greater than 0 dB. When R_o and C are small, the parasitic pole occurs at a frequency higher than the crossover frequency, and the amplifier is stable. This is generally not the case in most TIA circuits, however, so we must find a way to compensate for the inverting input parasitic capacitance.

Adding a Feedback Capacitor (a Brief Digression)

A CFA with a single-pole transfer function, as given in Equation 3, is stable with any value of feedback resistor because the lagging phase shift around its feedback loop is limited to −90°. The secondary poles of real CFAs will introduce significant phase lag at high frequencies, however, which places a practical limit on the minimum value of R_F to ensure stability (45° is often the minimum acceptable phase margin). From here on, Z(s) will include a high-frequency pole at $s = p_H$, along with the dominant pole $s = p$.

To ensure that the feedback impedance does not go to zero, common advice says that we shouldn't use a feedback capacitor in any CFA circuit. It's not that simple, however, since the feedback capacitor introduces phase shift, in addition to magnitude changes. This section looks at what happens when a feedback capacitor is added to a CFA-based TIA, omitting the parasitic input capacitance for the moment. Adding a feedback capacitor, C_F, across the feedback resistor, R_F, in the circuit shown in Figure 2 produces a pole and a zero in the loop gain. Z_F is defined as the parallel combination of R_F and C_F:

$$Z_F = \frac{1}{C_F \left(s + \dfrac{1}{R_F C_F} \right)} \tag{8}$$

If R_F in Equation 2 is replaced with Z_F, then the closed-loop gain is as expressed in Equation 9.

$$\frac{v_o}{i} = \left[\frac{1}{C_F \left(s + \dfrac{1}{R_F C_F} \right)} \right] \left[\frac{1}{1 + \dfrac{R_O \left(s + \dfrac{1}{(R_O \| R_F) C_F} \right)}{Z(s) \left(s + \dfrac{1}{R_F C_F} \right)}} \right] \tag{9}$$

The loop gain is then

$$\text{Loop Gain} = \frac{Z(s) \left(s + \dfrac{1}{R_F C_F} \right)}{R_O \left(s + \dfrac{1}{(R_O \| R_F) C_F} \right)} = \left(\frac{Z_O}{R_O} \right) \frac{\left(s + \dfrac{1}{R_F C_F} \right)}{\left(1 - \dfrac{s}{p} \right) \left(1 - \dfrac{s}{p_H} \right) \left(s + \dfrac{1}{(R_O \| R_F) C_F} \right)} \tag{10}$$

The loop gain has a dominant pole at $s = p$ and a high-frequency pole at $s = p_H$ from Z(s). In addition, it has a pole at $s = -\dfrac{1}{(R_O \| R_F) C_F}$ and a zero at $s = -\dfrac{1}{R_F C_F}$ due to the added feedback capacitor.

In the Bode plot, the zero due to C_F occurs at a lower frequency than the pole due to C_F because the zero frequency expression contains R_F in the denominator, and the pole frequency expression contains $(R_o || R_F)$ in the denominator. The Bode plot for one possible CFA-based TIA with C_F (Equation 10) is shown in Figure 4.

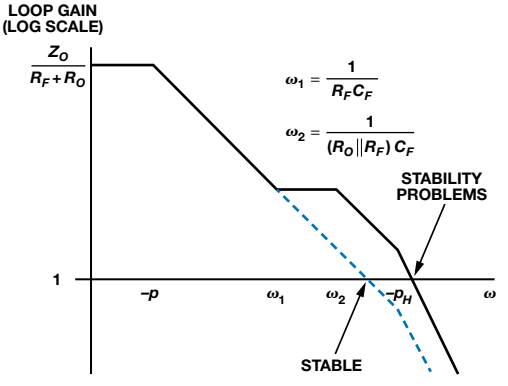

Figure 4. Bode plot of CFA-based TIA with feedback.

The zero produces increasing magnitude and leading phase shift with increasing frequency, which can, in some situations, be a good thing from a stability standpoint. In the system modeled in Figure 4, however, the zero pushes out the point where the loop gain crosses 0 dB, and the pole at p_H causes the magnitude asymptote to drop at −40 dB/decade beyond crossover. The dashed blue line shows the loop gain without C_F, using Equation 2 and the two-pole version of Z(s), as expressed in Equation 11.

$$\text{Loop Gain without } C_F = \frac{Z_O}{R_F + R_O} \left(\frac{1}{\left(1 - \dfrac{s}{p} \right) \left(1 - \dfrac{s}{p_H} \right)} \right) \tag{11}$$

Figure 4 shows that the amplifier is stable without C_F but develops stability problems when C_F is added. The plot in Figure 4 does not completely preclude the use of a feedback capacitor, as this particular Z(s) is not representative of all CFAs and actual resistor and capacitor values are not used, but it does show that the high-frequency pole limits how much feedback capacitance can be safely applied. Figure 4 also shows that any amount of feedback capacitance could be safely added to a hypothetical CFA with a single-pole transfer function and that adding the feedback capacitance would extend its closed-loop bandwidth.

Using the Zero Due to C_F to Cancel the Pole Due to the Parasitic Capacitance

Now that the effect of adding C_F to a CFA is understood in a general sense, it can be shown that C_F can be safely used to compensate for the parasitic shunt capacitance of an input current source.

The closed-loop gain of the circuit in Figure 3 is indicated in Equation 6. In order to see what happens to this circuit when a feedback capacitor is added, R_F can be replaced by Z_F in Equation 6, similar to what was done to develop Equation 9, where Z_F is defined in Equation 8. The circuit is shown in Figure 5.

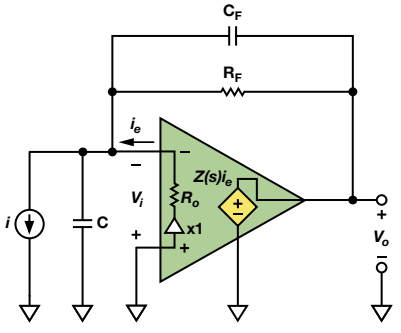

Figure 5. Practical CFA-based TIA with C_F used to compensate parasitic capacitance.

The closed-loop gain of the circuit in Figure 5 is given in Equation 12.

$$\frac{v_o}{i}=\left[\frac{1}{C_F\left(s+\frac{1}{R_FC_F}\right)}\right]\left[\frac{1}{1+\frac{R_o(C+C_F)\left(s+\frac{1}{(R_F\|R_o)(C+C_F)}\right)}{Z(s)C_F\left(s+\frac{1}{R_FC_F}\right)}}\right] \quad (12)$$

from which the loop gain can be determined to be

$$\text{Loop Gain with } C \text{ and } C_F = \frac{Z(s)C_F\left(s+\frac{1}{R_FC_F}\right)}{R_o(C+C_F)\left(s+\frac{1}{(R_F\|R_o)(C+C_F)}\right)} =$$

$$\left(\frac{Z_OC_F}{R_o(C+C_F)}\right)\frac{\left(s+\frac{1}{R_FC_F}\right)}{\left(1-\frac{s}{p}\right)\left(1-\frac{s}{p_H}\right)\left(s+\frac{1}{(R_F\|R_o)(C+C_F)}\right)} \quad (13)$$

The zero due to CF in Equation 13 is the same as the zero in Equation 10, but the pole due to CF has moved from

$$s=-\frac{1}{(R_O\|R_F)C_F} \text{ to } s=-\frac{1}{(R_O\|R_F)(C+C_F)}.$$

The addition of C to C_F allows the pole position to be moved to match the zero position, thus canceling out the pole due to the parasitic capacitance, C, of the input current source. Setting the pole frequency due to C_F and C equal to the zero frequency due to C_F in Equation 13 yields Equation 14:

$$\frac{1}{R_FC_F}=\frac{1}{(R_F\|R_o)(C+C_F)}\Rightarrow C_F=\left(\frac{R_o}{R_F}\right)C \quad (14)$$

Equation 14 shows the simple formula to calculate the value of C_F, which cancels the pole in the loop gain due to the parasitic capacitance, C, in the TIA shown in Figure 5. With this perfect pole-zero cancellation, the loop gain reverts back to its original form with dominant and high-frequency poles as in Equation 11. The closed-loop gain can now be expressed as shown in Equation 15.

$$\frac{v_o}{i}=\left[\frac{1}{C_F\left(s+\frac{1}{R_FC_F}\right)}\right]\left[\frac{1}{1+\frac{R_F+R_O}{Z(s)}}\right] \quad (15)$$

The main difficulty encountered when using Equation 14 is determining R_o, which can be variable, and is not always specified in CFA data sheets. The pole-zero cancellation does not need to be exact, however, as long as the slope of the loop gain plot is reasonably close to –20 dB/decade as it passes through 0 dB. Equation 14 shows that C_F decreases linearly with R_o due to the increasing bootstrapping that occurs as R_o approaches 0, where C becomes fully bootstrapped and the required C_F equals 0. Equation 14 can also be expressed in a matched time constant form as $R_oC = R_FC_F$. The matched time constant form of Equation 14 bears a strong resemblance to the result obtained when compensating VFAs for parasitic summing node capacitance: $R_GC_G = R_FC_F$, where R_G is the VFA gain resistor and C_G is the capacitance across R_G, which is usually the parasitic summing-node capacitance. There is, however, a price to pay for this benefit. While adding C_F stabilizes the TIA, it also introduces a pole in the closed-loop gain at $s=-\frac{1}{R_FC_F}$, as can be seen in Equation 12 and Equation 15. The closed-loop gain described by Equation 15 can be thought of as two cascaded systems with their transfer functions multiplied together. The first system has the leftmost factor in Equation 15 as its transfer function and has dimensions of ohms. The second has the rightmost factor in Equation 15 as its transfer function and is dimensionless.

The response of the second system is governed by the loop gain and can be modeled by a first-order transfer function as long as the loop gain magnitude crosses 0 dB at –20 dB/decade. Basic feedback theory shows that if this roll-off condition is met, the closed-loop gain magnitude of the second system is approximately unity when the loop gain magnitude is >>1, and follows the loop gain magnitude when the loop gain magnitude is <<1. The 3-dB point in the closed-loop gain occurs at the frequency where the loop gain magnitude crosses 0 dB (if the slope is a little faster than –20 dB/decade, some peaking will occur in the closed-loop response near the 0-dB crossover point). In a stable amplifier, the second system can, therefore, be approximated as a first-order, low-pass filter with unity gain in the pass-band and cutoff frequency equal to the frequency, where the loop gain magnitude crosses 0 dB. The transfer function of the first system is the reciprocal of the feedback factor and has a simple first-order, low-pass response with a dc value of RF and corner frequency of $\frac{1}{2\pi R_FC_F}$.

Intuitively, the additional pole due to C_F makes sense because the output voltage is developed by current flowing through the feedback impedance, which decreases with increasing frequency. The pole forms where the reactance of C_F is equal to the value of R_F. This same situation occurs in VFA-based TIAs that use feedback capacitor compensation. The closed-loop bandwidth can, however, be broadened somewhat by cautiously decreasing C_F from the value calculated in Equation 14, moving the pole frequency out, and reducing phase margin, but this must be done experimentally.

Simulation Data

To test this result, a simple simulation model for a CFA was developed with $Z_o = 1\ M\Omega$, $p = -2\pi$ (100 kHz), $p_H = -2\pi$ (200 MHz), $R_o = 50\ \Omega$, and $R_F = 500\ \Omega$. The magnitude of the loop gain is found by taking the magnitude of Equation 11 with these values.

$$\left|\text{Loop Gain without } C_F\right| = \frac{10^6}{500+50}\left(\frac{1}{\sqrt{1+\left(\frac{f}{100\text{ kHz}}\right)^2}\sqrt{1+\left(\frac{f}{200\text{ MHz}}\right)^2}}\right) \quad (16)$$

which equals 1 at approximately $f = 145$ MHz.

The loop gain phase shift at 145 MHz is given

$$\angle\text{Loop Gain without } C_F = -\tan^{-1}\left(\frac{145\text{ MHz}}{100\text{ kHz}}\right) - \tan^{-1}\left(\frac{145\text{ MHz}}{200\text{ MHz}}\right) \approx -126^\circ, \quad (17)$$

resulting in approximately 54° of phase margin, which is a reasonable place to start for a basic CFA with no parasitic capacitances.

Figure 6 shows the simulation of the response of this model to a 1-ns rise time current step input.

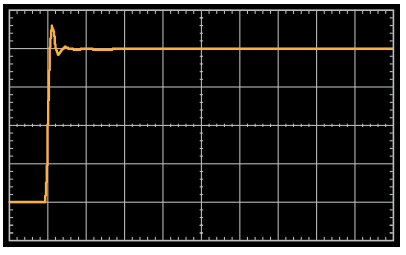

Figure 6. Basic TIA step response with no parasitic capacitance (20 ns/div).

The response is clean, with minimal ringing—just what would be expected with 54° of phase margin. The step response of the same amplifier with 50 pF of parasitic capacitance added between the inverting input and ground is shown in Figure 7.

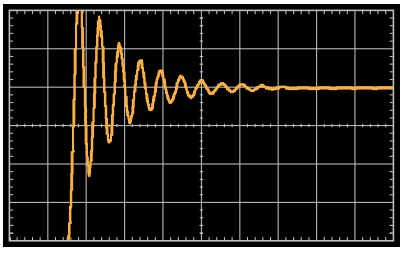

Figure 7. Step response with 50 pF of capacitance between inverting input and ground (20 ns/div).

The vertical scale in Figure 7 is the same as it is in Figure 6, but the trace was moved down one division to accommodate the ringing. The excessive ringing is clear, and this amplifier clearly has a phase margin problem.

The amplifier can be stabilized by adding a feedback capacitor determined by Equation 14, which is calculated to be 5 pF. Figure 8 shows the results when the 5-pF feedback capacitor is added.

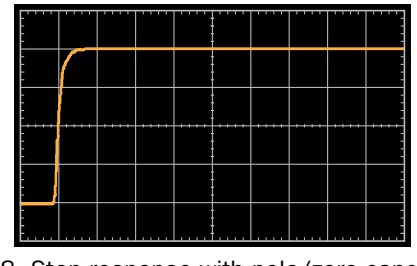

Figure 8. Step response with pole/zero cancellation using 5-pF feedback capacitance (20 ns/div).

The bandlimiting due to the pole in the closed-loop gain is evident. The loop gain 0-dB crossover for the original amplifier was determined to be 145 MHz, which corresponds to a time constant of approximately 1.1 ns in a first-order system, and the R_FC_F time constant is 2.5 ns (note that the loop gain magnitude roll-off rate is a little faster than –20 dB/decade at the 0-dB crossover since the phase margin is less than 90°, but the first-order, closed-loop model is a reasonably accurate approximation). Using the model of two cascaded systems as described above, the aggregate time constant of the cascaded systems can be estimated to be the root-sum-square of the two time constants (the input current source 10% to 90% rise time of 1 ns corresponds to an effective sub-ns time constant that is short enough to ignore), or approximately 2.7 ns, which looks about right for the response shown in Figure 7.

Reducing C_F to 3 pF reduces the phase margin somewhat and increases the closed-loop pole frequency, speeding things up as shown in Figure 9.

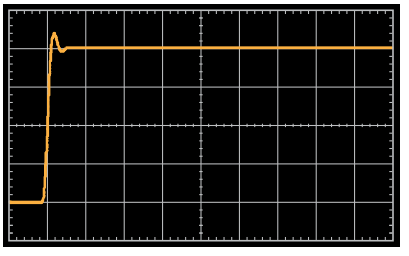

Figure 9. Step response with 3-pF feedback capacitance (20 ns/div).

It's clear that some experimentation may be necessary to get the best value for C_F. Other factors such as load capacitance, board layout, and variations in R_o also factor into the selection of C_F.

Conclusion

With the increasing interest in the use of CFAs as TIAs, it is important to understand how to compensate for transducer capacitance on a CFA's inverting input and why the compensation works. This article uses classical feedback techniques to develop a simple scheme that adds a single feedback capacitor in parallel with the feedback resistor to compensate for the inverting input capacitance. The feedback capacitor introduces an undesired pole in the closed-loop response, but the capacitor's value can be empirically adjusted from the calculated value to reduce the pole's band-limiting effect.

References

Gray, Paul R., and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, Inc., 1977.

Lundberg, Kent. "Feedback Control Systems." M.I.T. Course Notes.

Roberge, James K. *Operational Amplifier: Theory and Practice*. John Wiley & Sons, 1975.

Author

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Amplifier Disable Function Eliminates Need for Multiplexers in Multichannel Applications

By Charly El-Khoury

A *multiplexer* (mux) routes the signal from one of several inputs to a common output, allowing one device or resource—such as an ADC in a mixed-signal application or a display in a video application—to be shared, rather than dedicating a device to each input. Many applications use amplifiers to condition the signal before the multiplexer. In these cases, amplifiers with a disable function can be used to select the channel, eliminating the need for a multiplexer—and reducing cost, PCB area, and distortion. This article presents the challenges of using op amps with a disable function for channel selection and offers examples from ADI's high-speed amplifier portfolio.

First, it is important to compare the *disable* function with the *power-down* function. When an amplifier is disabled, the power consumption drops, and the output goes into a high-impedance state, allowing multiple outputs to be tied together. This differs from the power-down function, which is only intended to save power.

When using op amps to select channels, the second thing to consider is the maximum voltage allowed between the amplifier inputs. This information is usually found in the Absolute Maximum Ratings on the data sheet, as shown in Figure 1. If the amplifier has back-to-back diodes between its inputs, the differential input voltage will be limited—even when the amplifier is disabled—to 0.7 V, 1.2 V, or more depending on the number of series-connected back-to-back diodes.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	12.6 V
Internal Power Dissipation[2]	
PDIP Package (N)	1.3 W
SOIC Package (R)	0.9 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±3.4 V
Output Short-Circuit Duration	
	Observe Power Derating Curves
Storage Temperature Range N, R	–65°C to +125°C
Operating Temperature Range (A Grade)	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

Figure 1. AD8041 absolute maximum ratings.

Some amplifiers, such as the AD8041, do not have back-to-back diodes between their inputs, so they can handle differential input voltages of up to ±3.4 V. When disabled, the amplifier output is in a high-impedance state. Configured for a gain of 2, two amplifiers can be connected to select one of two channels while operating on a single 5-V supply, as shown in Figure 2.

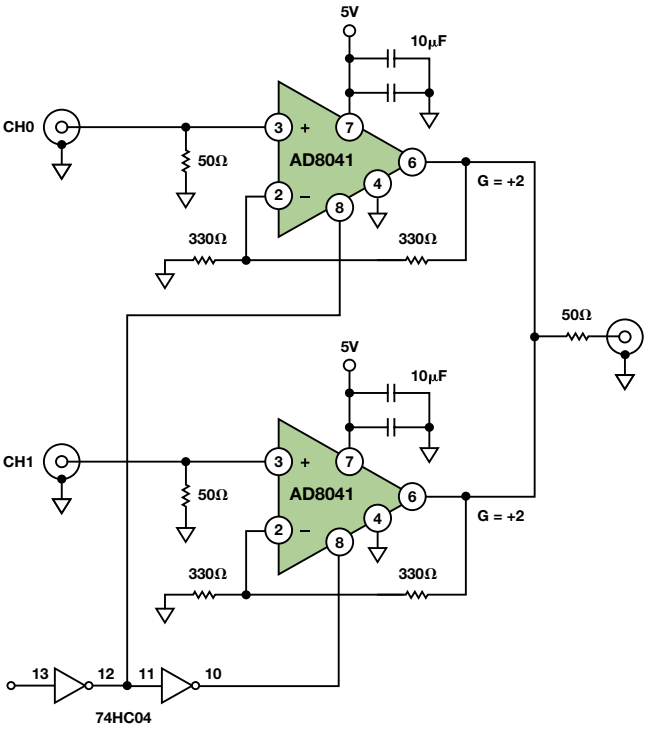

Figure 2. 2:1 multiplexer using two AD8041 op amps.

This is not true for all amplifiers with disable pins, however. To illustrate this, Table 1 shows some high-speed amplifiers with a disable function, along with their differential input voltage ratings, bandwidth, and minimum gain requirements.

Table 1. High-Speed Amplifiers with Disable Function

Part Number	# of Amps	Bandwidth (MHz)	Differential Input Voltage (V)	Minimum Stable Gain
AD8021	Single	490	±0.8	1
AD8027	Single	190	±1.8	1
AD8029	Single	125	±1.8	1
AD8041	Single	160	±3.4	1
AD8063	Single	320	±6	1
AD8099	Single	440	±1.8	2
ADA4853-1	Single	100	±5	1
ADA4895-1	Single	236	±0.7	10
ADA4897-1	Single	230	±0.7	1
ADA4899-1	Single	535	±1.2	1
AD8028	Dual	190	±1.8	1
ADA4853-2	Dual	100	±5	1
ADA4895-2	Dual	236	±0.7	10
ADA4897-2	Dual	230	±0.7	1
AD813	Triple	125	±6	1
AD8013	Triple	230	±6	1
AD8023	Triple	460	±3	1
ADA4853-3	Triple	100	±5	1

As an example, the ADA4897-2 dual low-power op amp with individual disable pins will be used for both signal conditioning and channel selection, eliminating the need for a multiplexer. Figure 3 shows a simple schematic of two unity gain buffers configured as a 2:1 channel selector. Three scenarios will be analyzed: 1) two input sources, CH0 and CH1, have a 2.5-V dc level and a 0.5-V p-p ac signal; 2) same signals but with a 1-V dc offset between the two input sources; and 3) same dc level with a 1-V p-p ac signal. Due to the back-to-back diodes between the inverting and noninverting inputs of each amplifier, the differential input voltages should not exceed 0.7 V.

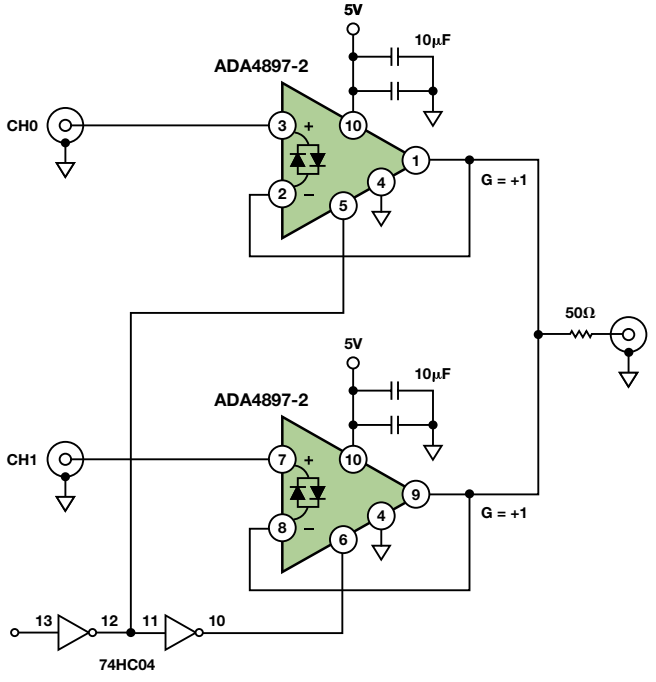

Figure 3. 2:1 multiplexer using the dual ADA4897-2.

When an amplifier is enabled, the feedback forces the inverting and noninverting inputs to be equal, but when the amplifier is disabled, the feedback loop is opened, and the inputs can drift apart. With back-to-back diodes between the two inputs, the amount they can drift apart is limited. In the case of the ADA4897-2, the inputs cannot drift apart by more than a diode drop (0.7 V), or the back to-back diodes will turn on. To help illustrate this point, Figure 4 shows a simplified schematic of the circuit with one amplifier disabled.

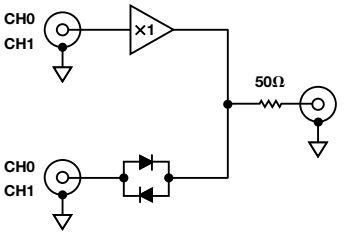

Figure 4. Simplified schematic of Figure 3 with one amplifier disabled.

Returning to our three scenarios, if the dc levels on CH0 and CH1 are equal, the maximum differential ac signal that can exist between the two input sources is 0.7 V before the diodes become forward-biased. The first scenario will work as expected because the maximum differential signal is only 0.5 V p-p. In the second scenario, the two input sources have a dc offset level greater than 0.7 V, so the circuit will not work. In the third scenario, the maximum differential signal could reach 1 V p-p when the two input sources are 180 degrees out of phase. This will cause the back-to-back diodes to become forward-biased, so the circuit will not work under these conditions either. Using the AD8041 or other amplifier (from Table 1) with a large enough differential input voltage would be a better option for the last two scenarios.

If an amplifier with back-to-back diodes must be used due to cost or performance considerations, and adding an extra multiplexer is not an option, setting the amplifier for a gain greater than 1, or using feedback resistors in the unity-gain configuration, can make the problem less severe. The second option is only an issue with voltage feedback amplifiers, as they are not meant to use a feedback resistor for unity gain. If peaking is a problem, however, a capacitor, in parallel with the feedback resistor, can reduce the peaking and minimize the effects of the feedback resistor.

Figure 5 shows a simplified schematic of Figure 2, but using the ADA4897-2 instead of the AD8041. The amplifiers are configured for a gain of 2.

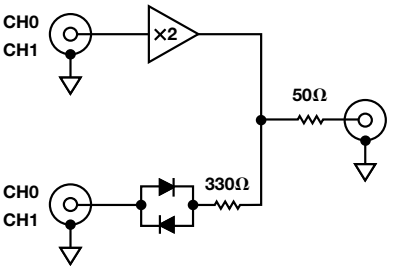

Figure 5. Simplified schematic of Figure 2 with ADA4897-2.

In this circuit, the feedback resistor limits the current that can flow through the back-to-back diodes. This keeps the diodes from becoming completely forward-biased and loading the circuit. If, for example, CH0 and CH1 were 1 V p-p, the maximum differential signal across the resistor (assuming 0.7-V diode drop) would be 1.5 V – 0.7 V = 0.8 V, which corresponds to a current of 0.8 V/330 Ω = 2.4 mA. This worst case current is low enough compared to the load current, so the amplifier should be able to provide it while driving the rest of the circuit. Increasing the value of the feedback resistor will reduce the current, if necessary. Using a gain of 2 instead of unity gain (or using feedback resistors in unity gain, assuming the voltage feedback amplifier is stable in this configuration) allows double the ac input voltage. When using feedback and gain resistors, the offset dc voltage level between CH0 and CH1 can be canceled by adding a dc bias to the inverting input. In high-precision applications, it might be better to use amplifiers without back-to-back diodes because the diodes might distort the signal, even if they are not fully on.

In conclusion, using amplifiers with a disable function as channel selectors is possible as long as all input back-to-back diodes remain unsaturated. A unity-gain configuration is more limited than higher gains, where the gain and feedback resistors can be used to limit current flow through the back-to-back diodes and eliminate the dc bias. If unity gain is required, resistors can be used in the feedback loop as long as the amplifier is stable in this configuration. Finally, keep in mind that back-to-back diodes can cause distortion, so amplifiers without back-to-back diodes might be a better choice for high-precision applications.

Author

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Minimizing Errors in Multiplexed 3-Wire RTD Data-Acquisition Systems

By Henry He

Resistance temperature detectors (RTDs) monitor temperature in many industrial applications. In a distributed control system (DCS) or programmable logic controller (PLC), one data-acquisition module may monitor the temperature of many remotely located RTDs. In high-performance applications, the best accuracy will be obtained when each RTD has its own excitation circuit and ADC, but the data-acquisition module will be large, expensive, and power hungry. Multiplexing leads to a smaller, lower cost, lower power module, but some accuracy can be lost. This article discusses how to minimize errors in a multiplexed system.

Circuit Structure

RTDs are available in 2-wire, 3-wire, and 4-wire configurations, where 2-wire devices are the least expensive and 4-wire devices are the most accurate. Commonly used in industrial applications, 3-wire RTDs can be excited by two identical current sources to cancel out lead resistance. When used with a precision reference resistor, current source errors do not affect the measurement accuracy. High-performance ADCs, such as the AD7792 and AD7793, integrate the excitation current sources, making them ideal for high-accuracy RTD measurements.

Figure 1 shows two 3-wire RTDs excited by the on-chip current sources. The RTD channel is selected by a multiplexer, such as the ADG5433 high-voltage, latch-up proof, triple SPDT switch.

Only one RTD can be measured at one time. S1A, S1B, and S1C are closed to measure RTD #1; S2A, S2B, and S2C are closed to measure RTD #2. A single ADG5433 can switch two 3-wire RTDs; additional multiplexers can be added to handle more than two sensors. RL_{XX} represents the resistance introduced by long wires between the RTD and the measurement system, plus the *on* resistance of the switches.

Calculating the RTD Resistance

With S1A, S1B, and S1C closed to measure RTD #1, the resistance of the RTD can be calculated as follows:

$$\text{Define } \Delta V_{IN} = V_{IN+} - V_{IN-}$$

$$\text{Assume } I_{OUT1} = I_{OUT2} = I_{OUT} \text{ and } RL_{1A} = RL_{1B} = RL_{1C}$$

$$I_{OUT1} + I_{OUT2} \text{ flows through } R_{REF}, \text{ so } I_{OUT1} = \frac{V_{REF}}{2R_{REF}}$$

$$RTD = \Delta V_{IN} / I_{OUT} = \frac{\Delta V_{IN} \times 2R_{REF}}{V_{REF}}$$

Thus, the measurement depends only on the value (and accuracy) of R_{REF}. Remember, however, that we assumed $I_{OUT1} = I_{OUT2}$ and $RL_{1A} = RL_{1B} = RL_{1C}$. In fact, mismatches in these currents and resistances are the main source of measurement error.

Impact of Mismatched Current Sources and Wire Resistors

Next, assume that the two current sources are mismatched, such that $I_{OUT2} = (1 + x)\, I_{OUT1}$. Now, consider the following:

$$RTD = \frac{\Delta V_{IN}}{V_{REF}}(2 + x)R_{REF} + (1 + x)RL_{1C} - RL_{1A}$$

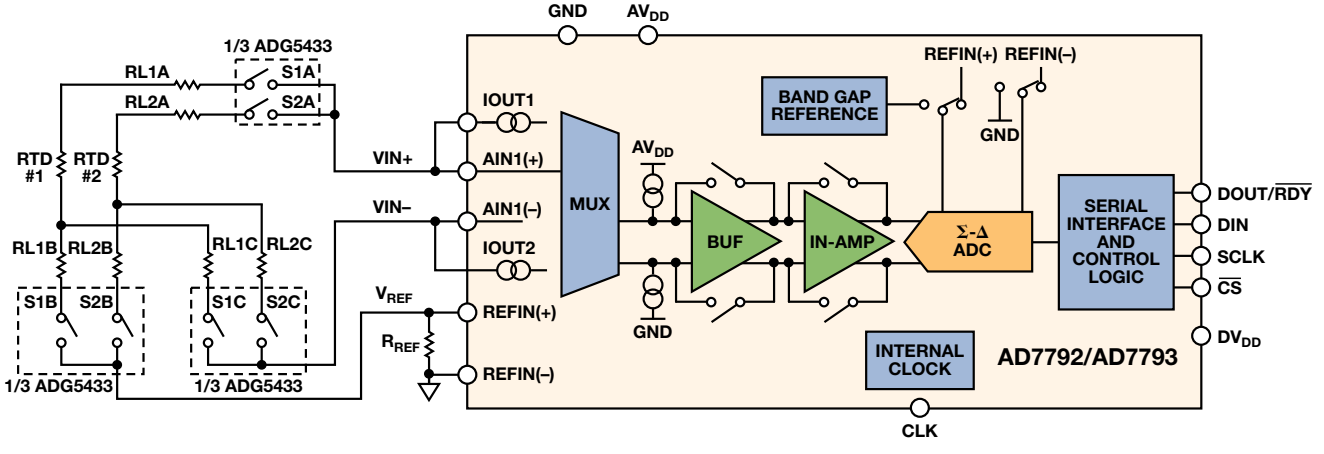

Figure 1. Two 3-wire RTDs multiplexed into one AD7792/AD7793 ADC.

Note that the mismatch creates both an offset error and a gain error. The offset error is related to the mismatch between the two lead resistances, while the gain error is related to the mismatch between the two current sources. If these mismatches are not taken into consideration, the calculated value of the RTD resistance, based on the data read from the ADC, will be incorrect.

Using a 200-Ω RTD as an example, Table 1 shows the acquired values when the mismatches are not considered, given R_{REF} = 1000 Ω, I_{OUT1} = 1 mA, $I_{OUT2} > I_{OUT1}$ by the percentage shown, RL_{1A} = 10 Ω, and $RL_{1C} > RL_{1A}$ by the resistance shown.

Table 1. Measured RTD Values When Mismatches Are Not Considered

$(I_{OUT2} - I_{OUT1})/I_{OUT1}$ \ $RL_{1C} - RL_{1A}$	0.01 Ω	0.1 Ω	1 Ω
0.1%	199.88	199.79	198.89
0.5%	199.44	199.35	198.45
1.0%	198.90	198.81	197.90

Minimizing the Errors

The data shows that small mismatches will degrade the accuracy severely, and that well matched current sources and switches should be used to improve performance.

The transfer function is linear, so initial errors due to current source and resistance mismatches can be calibrated out easily. Unfortunately, the mismatch varies with temperature, making it difficult to compensate. Hence, it's important to use devices that have low drift over temperature.

With $I_{OUT1} \neq I_{OUT2}$, and the current sources connected as shown:

$$\Delta V_{IN1} = I_{OUT1}\,(RL_{1A} + RTD) - I_{OUT2} \times RL_{1C}$$

Assume we swap I_{OUT1} and I_{OUT2}, so that I_{OUT1} now connects to V_{IN-} and I_{OUT2} now connects to V_{IN+}:

$$\Delta V_{IN2} = I_{OUT2}\,(RL_{1A} + RTD) - I_{OUT1} \times RL_{1C}$$

Now, if we sum the results from a conversion with the current sources connected in the original orientation and a second conversion with the current sources swapped, the result is

$$\Delta V_{IN1} + \Delta V_{IN2} = (I_{OUT1} + I_{OUT2}) \times (RTD + RL_{1A} - RL_{1C}) = \frac{V_{REF}}{R_{REF}}\,(RTD + RL_{1A} - RL_{1C})$$

$$\text{Consequently, } RTD = \frac{\Delta V_{IN1} + \Delta V_{IN2}}{V_{REF}} \times R_{REF} + RL_{1C} - RL_{1A}$$

Note that the measurement is now independent of current source mismatch. The only downside is the loss of speed, because two conversions are needed for each RTD calculation.

The AD7792 and AD7793 are designed for this application. As shown in Figure 2, integrated switches make it easy to swap the current sources to the output pins by writing to an I/O register.

Conclusion

Swapping the excitation current sources within the AD7792/AD7793 can improve accuracy in a multiplexed RTD measurement circuit. Calculations show the importance of mismatches between current sources and wire resistances.

References

Kester, Walt, James Bryant, and Walt Jung. "Temperature Sensors." *Sensor Signal Conditioning*, Section 7. Analog Devices, Inc., 1999.

Author

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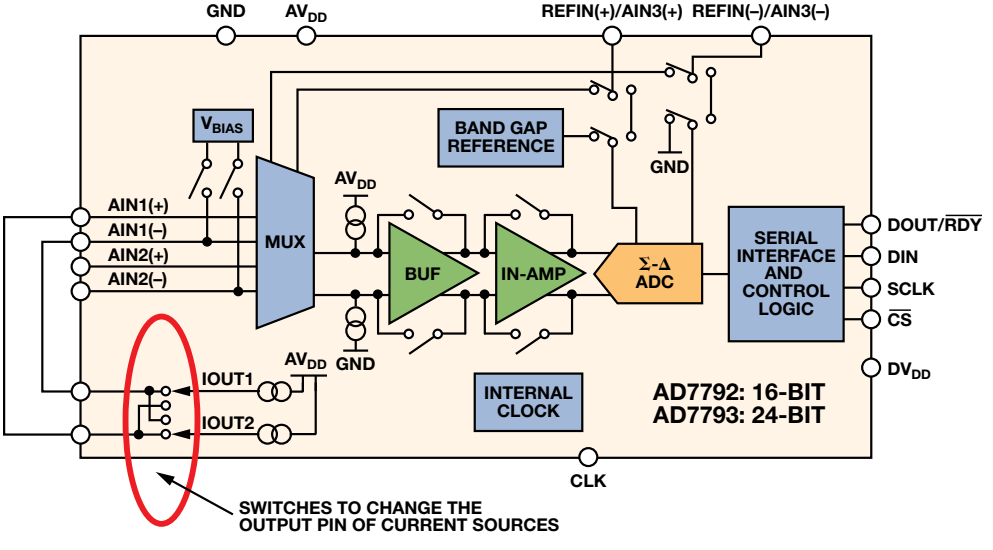

Figure 2. Functional block of AD7792/AD7793.

System Demonstration Platform Eases Transition from Evaluation to Prototyping

By Rosemary Ryan

Introduction

To simplify the process of selecting components for new designs, Analog Devices provides design engineers with *evaluation boards* and *application software*. After the initial evaluation has been completed, a few aspects of the design typically require further investigation. How will the component hook up to the system's FPGA, microcontroller, or digital signal processor (DSP)? Can the interface and application code be verified before finalizing the system design? Can HDL coding be started while waiting for a printed circuit board to arrive? The best way to save time and increase the chance of success is to have the code and interface ready before the board is built. While the *System Demonstration Platform* (SDP) from Analog Devices is primarily an evaluation tool, it was designed to allow this type of prototyping, making it simpler than ever to kick start system development.

System Demonstration Platform

The low cost, reusable SDP evaluation platform, shown in Figure 1, was designed with versatility in mind. Comprising *controller boards*, *interposer boards*, and *daughter evaluation boards*, the platform facilitates quick, easy movement from evaluation to prototyping.

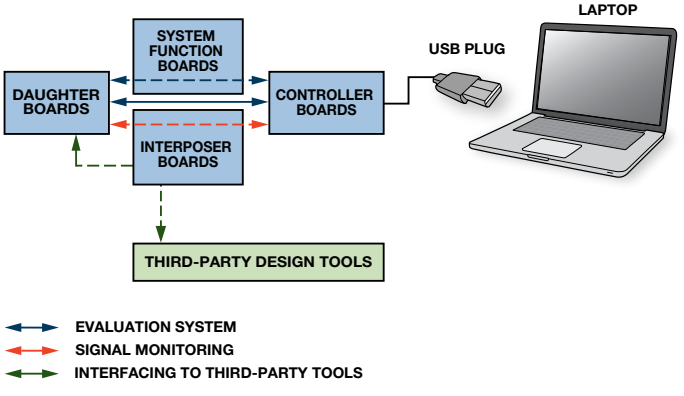

Figure 1. System demonstration platform overview.

The two-board evaluation system includes a controller board that can be reused with multiple daughter boards. The controller board connects to a personal computer over USB 2.0 and provides the daughter board with a series of commonly used communication interfaces through a standard 120-pin connector. Over 180 compatible boards for *product evaluation* and *reference circuit evaluation* are available, all with the same 120-pin connector, which also connects to the input and output signals of the component being evaluated. The full range of product evaluation boards includes those for ADCs, DACs, DDS, RF PLLs, and MEMS microphones. Reference circuit evaluation boards are available for all applications in which ADI components are used, including automotive, healthcare, process control, and industrial automation. Figure 2 shows the SDP-B controller board connected to a PulSAR® ADC evaluation board. A complete list of available boards can be found at www.analog.com/sdp.

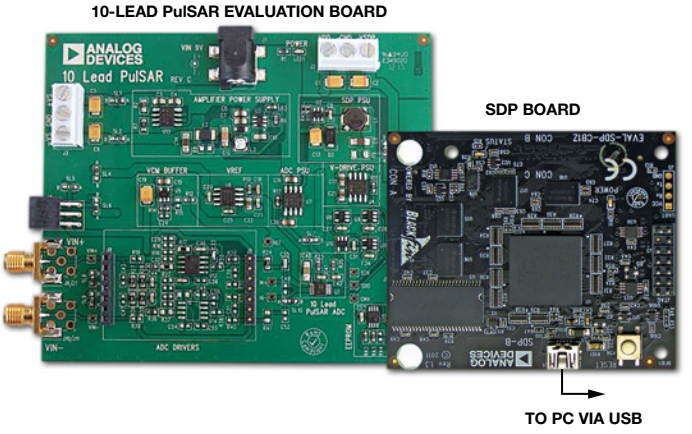

Figure 2. Evaluation hardware setup with the SDP-B and a PulSAR ADC evaluation board.

The platform also includes a series of interposer boards that allow the wide range of daughter boards to connect directly to third-party evaluation tools, such as Xilinx® FPGA evaluation boards or the BeMicro Software Development Kit (SDK). These interposer boards, which connect the inputs and outputs of the component on the ADI evaluation board to a Xilinx or Altera® FPGA, are the key that enables quick, easy prototyping with ADI evaluation boards and third-party tools.

120-Pin Connector

The 120-pin connector uses the same standard, well-defined pinout as ADI's DSP EZ-KIT Lite.® The connector includes SPI, I^2C, SPORT, GPIO, timers, and parallel interfaces, plus power and ground pins. The connector supports 3.3-V logic levels.

Interposer Boards

Interposer boards connect to a daughter board through the standard 120-pin connector. They then route the signals from the 120-pin connector to a second connector, allowing the user to connect the daughter board to their choice of FPGA evaluation board. Interposer boards, which do not include any additional logic or signal conditioning, simply route signals from the SDP connector to the second connector—the VITA 57 standard FMC connector, for example. Three interposer boards are available, including the SDP-I-FMC interposer, BeMicro SDK/SDP interposer, and SDP breakout board.

SDP-I-FMC Interposer

The SDP-I-FMC interposer, shown in Figure 3, connects any SDP-compatible evaluation board to a Xilinx FPGA evaluation board that supports 3.3-V I/O. It includes the standard 120-pin connector and a low-pin-count (LPC) FMC connector, which is part of the industry-standard VITA 57 specification that outlines I/O connectivity to FPGAs. The 120-pin connector on the daughter board connects to the 120-pin receptacle on the SDP-I-FMC interposer. The FMC connector on the SDP-I-FMC interposer then connects to the FMC connector of the Xilinx evaluation board.

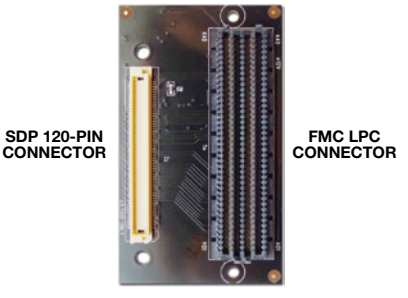

Figure 3. SDP-I-FMC interposer.

The Kintex KC705 is an example of a Xilinx evaluation board that has 3.3-V I/O and the FMC connector. Therefore, it can connect to an ADI evaluation board through the SDP-I-FMC, as shown in Figure 4. Example code for a large number of SDP-compatible evaluation boards is available on the ADI wiki site, allowing users to start their FPGA development as early as possible. Further details on the SDP-I-FMC, including a schematic and ordering information, can be found at www.analog.com/sdpFMC. The board retails for $49.

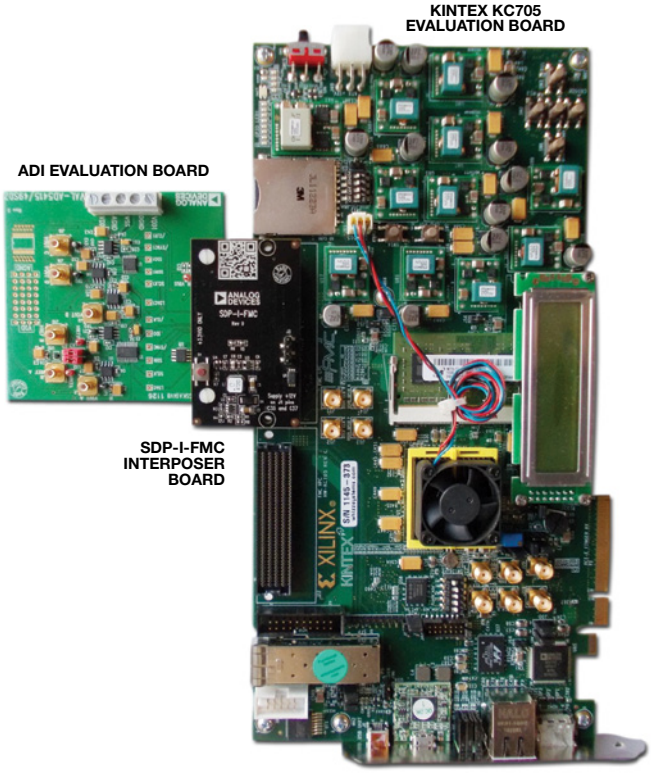

Figure 4. SDP-I-FMC interposer connects daughter board to Kintex KC705 evaluation board.

BeMicro SDK/SDP Interposer

The BeMicro SDK/SDP interposer, shown in Figure 5, allows users to connect a daughter board to an Altera Cyclone IV FPGA on the BeMicro SDK evaluation board. The BeMicro SDK/SDP interposer has the standard 120-pin connector to connect to ADI evaluation boards and a BeMicro edge connector receptacle to connect to the BeMicro SDK. The signals from the SDP connector are routed to the edge connector receptacle. The BeMicro SDK/SDP interposer can be purchased for $50 from www.arrownac.com (component name: ADI interposer). A schematic and other information can be found at www.analog.com/bemicroSDP.

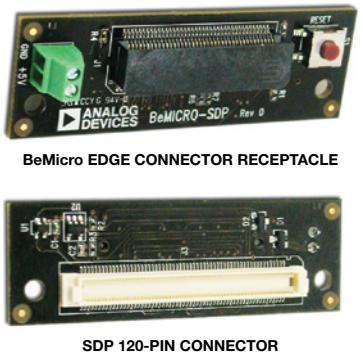

Figure 5. BeMicro SDK/SDP interposer.

BeMicro SDK

The BeMicro SDK is an Altera Cyclone IV-based hardware evaluation platform for creating, compiling, running, and debugging embedded software with the NIOS II processor. Developed by Arrow, in conjunction with Altera, it provides a small, low cost, easy to use FPGA evaluation and development platform. BeMicro SDK example projects for a large number of SDP-compatible evaluation boards are available at wiki.analog.com/resources/alliances/altera. An excellent starting point, the many available component interface examples can decrease FPGA system development time.

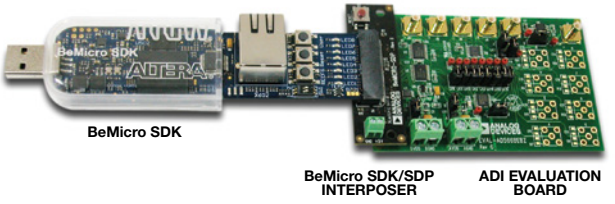

Figure 6. BeMicro SDK/SDP interposer connects daughter board to BeMicro SDK.

SDP Breakout Board

The SDP breakout board has four 120-pin connectors. Two (J1 and P1) are used with the SDP and SDP-compatible evaluation boards; and two (J2 and P2) are used with the ADSP-BF60x EZ-KIT.® The primary use of this board is signal monitoring. Each probe point represents a pin on the connector, allowing an oscilloscope to monitor activity on that pin. The board is also an effective tool for prototyping when dedicated interposer board hardware does not exist.

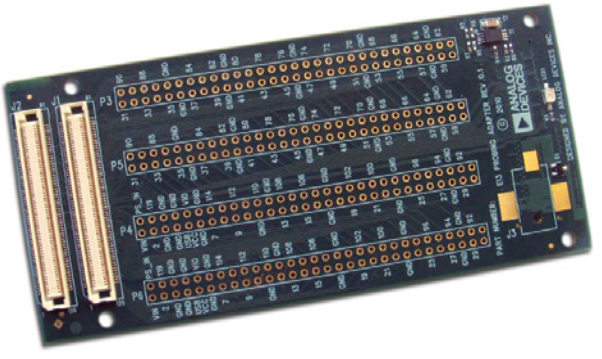

Figure 7. SDP breakout board.

The board has four rows of through-hole probe points, as shown in Figure 8. These can be easily wired to a DSP or microcontroller evaluation board. The signals from J1 and J2 are routed to P1 and P2, which are on the bottom of the SDP breakout board.

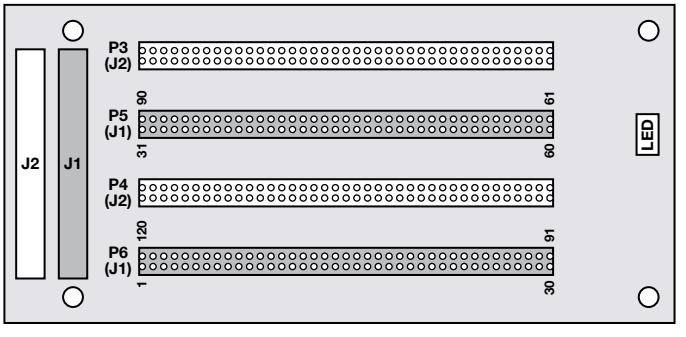

Figure 8. Top view of SDP breakout board.

(continued on Page 14)

Reduced Integration Time Improves Accuracy in Dead Reckoning Navigation Systems

By Ben Wang

An automotive *dead reckoning* (DR) navigation system uses a gyroscope (gyro) to estimate the vehicle's instantaneous heading. This information, combined with the distance traveled, allows the navigation system to correctly determine the vehicle's position, even when the satellite signal is blocked in a crowded downtown area or a tunnel. A major challenge to using a gyro in DR navigation is that the satellite signal may be lost for a long time, causing the accumulated angle error to become too large to accurately position the vehicle. This article offers a simple way to solve this problem.

How DR Navigation Works

Figure 1 shows the basic operation of DR navigation. A gyro measures the vehicle's rotation rate in degrees per second. The angle, which represents the vehicle's instantaneous heading, is calculated by integrating the rotation rate over time. Combining the heading and distance traveled allows the vehicle's position to be determined, as indicated by the red line.

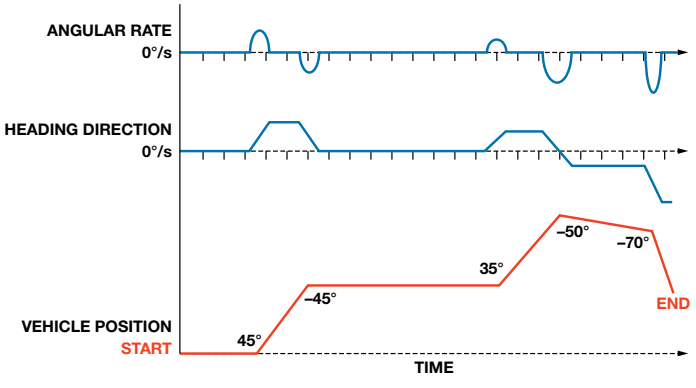

Figure 1. How DR navigation works.

With a digital gyro, the integrated rate can be expressed as the sum of rate samples multiplied by the sampling interval:

$$\text{angle} = \sum_{i=1}^{n} r_i \times \tau$$

where r_i is rate sensed by the gyro, n is the number of samples, and τ is the sampling interval.

The angular error accumulated over time can be expressed as:

$$\text{angular error} = \sum_{i=1}^{n} e_i \times \tau$$

where e_i is rate error for each sample, n is the number of samples, and τ is the sampling interval.

According to the formula, as the required integration time gets longer, the accumulated error gets bigger, as shown in Figure 2. These rate samples, measured using an evaluation board with the ADXRS810 high-performance angular rate sensor, simulate a DR navigation system with 3300 total rate samples recorded. The blue line shows the gyro rate samples; the red line shows the accumulated angular error. It is obvious that the accumulated angular error increases with time.

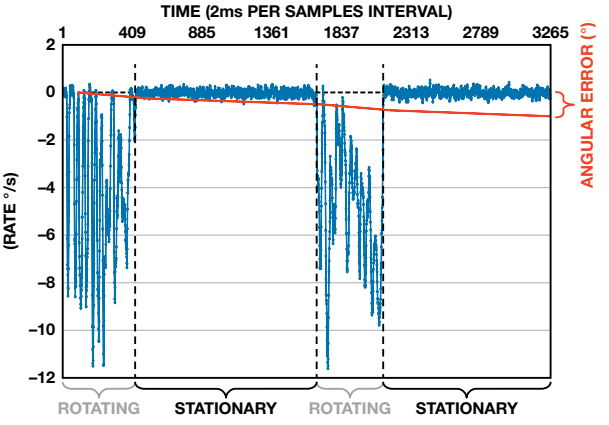

Figure 2. Rate measured using ADXRS810 evaluation board. (Note: angular error is not to scale.)

Using a Low-Pass Filter (LPF) to Reduce Integration Time

The traditional method to reduce angular error focuses on minimizing e_n, but today's digital gyros already have very low rate error specifications. The ADXRS810, for example, features 80 LSB/°/sec sensitivity, ±2°/sec offset, and 0.03°/sec/*g* shock immunity, leaving limited room for improvement. In addition, the algorithm to compensate e_n is complicated. Compared to other applications, such as electronic stability control (ESC), for example, the gyro in a DR navigation system can run for long periods of time, as would be the case when the GPS signal is lost as the vehicle travels through a long tunnel. Longer running time causes the accumulated angular error to be more significant in DR navigation applications.

If the integration time could be reduced, it would significantly decrease the accumulated angular error. When the gyro is not rotating, the rate output is small, but nonzero, due to gyro noise. The ADXRS810 achieves very low gyro noise and very high sensitivity, making it easy to filter out noise in the digital domain simply by setting the appropriate threshold. This process is equivalent to low-pass filtering, as the gyro rate noise is at a high frequency compared to the rate output due to rotation.

Figure 3 shows the LPF version of Figure 2, where all rate samples less than 1°/s are zeroed and, therefore, ignored when doing rate integration. The remaining integration time, considered effective integration time, is only about 16% of the total integration time. This provides a significant reduction of integration time. As a result, the accumulated angular error is also significantly reduced, as indicated by the red line.

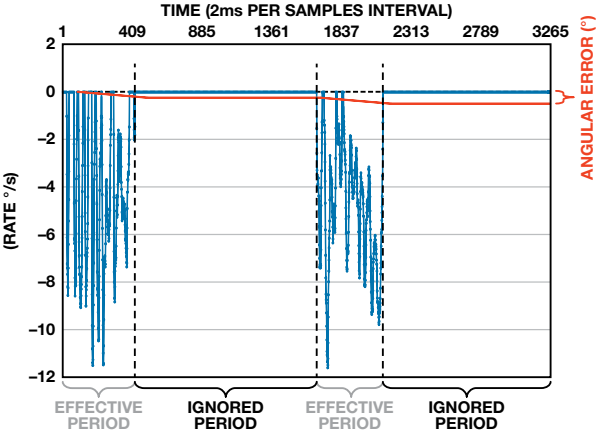

Figure 3. Rate measured using ADXRS810 evaluation board and digital LPF. (Note: angular error is not to scale.)

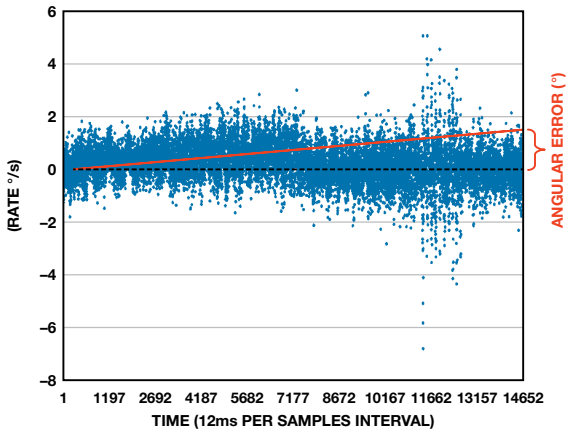

Figure 4. Unfiltered in-vehicle gyro rate samples. (Note: angular error is not to scale.)

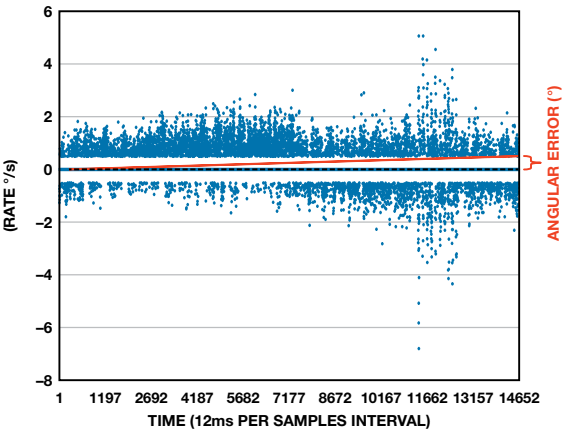

Figure 5. In-vehicle gyro rate samples after LPF. (Note: angular error is not to scale.)

In a practical application, the vehicle steering wheel is normally positioned at zero degrees. Thus, the effective integration time for gyro rates can be reduced by ignoring it, just as was done in the experiment described in Figure 3. Figure 4 shows gyro rate samples from a real in-vehicle test. Traveling through a tunnel for about 180 sec, it requires 180 sec for rate integration. Without the LPF process, the accumulated error over 180 sec can be up to 4°, which is too big to correctly determine the vehicle's location in the tunnel. By implementing the LPF process with a 0.5°/sec threshold, the effective integration time is reduced to only 84 sec, a reduction of about 53%. The accumulated error drops to about 0.5°, as shown in Figure 5. The LPF threshold can be set to achieve the accuracy required for the specific application.

Conclusion

Today's digital gyroscopes have excellent specifications, so the room to improve performance is quite limited. In vehicle DR navigation systems and other applications that require long integration times, setting an LPF threshold to reduce integration time is a simple but also effective method to improve accuracy.

The ADXRS810 high-performance, low-cost digital gyro uses ADI's innovative MEMS technology, making it a good choice for vehicle DR navigation applications. Housed in a very small package, it provides low offset, low noise, and high rate sensitivity. Temperature compensated on chip, it eliminates the need for an external temperature sensor and eases the algorithm for temperature compensation. Its high immunity to shock and vibration is very important in automotive applications.

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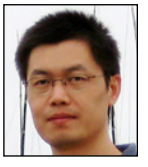

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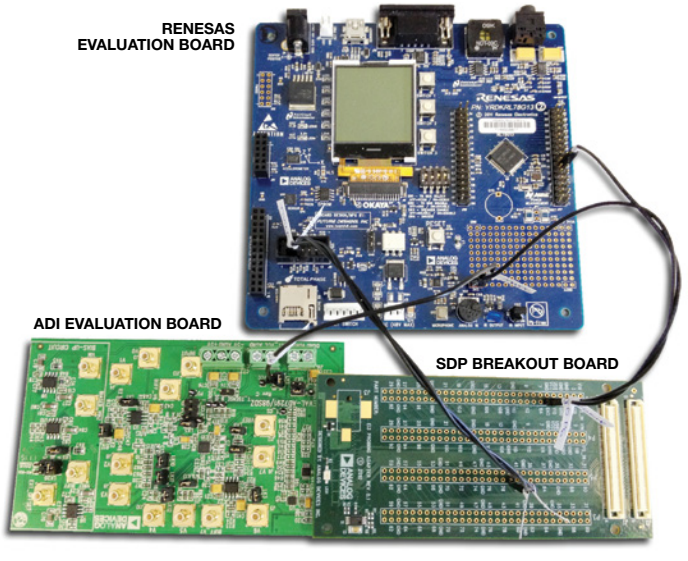

Figure 9. SDP breakout board connects the AD7291 evaluation board to Renesas evaluation board.

In the example setup, shown in Figure 9, the SPI pins of the SDP breakout board are wired to the Renesas RL78 evaluation board. The example code, available on the wiki site for many component evaluation boards, can be found via links on individual product pages on www.analog.com or in the microcontroller examples section of the ADI wiki.

Further details on the SDP breakout board, including the schematic and ordering information, can be found at www.analog.com/EI3Breakout. The board retails for $49.

Conclusion

Many options are available to help speed the design process when moving from evaluation to prototyping. With dedicated hardware, customizable hardware, and example code, ADI provides a range of solutions to meet a wide variety of needs. The System Demonstration Platform is constantly evolving, so we encourage your feedback regarding the prototyping hardware and software that would be most helpful to your design process.

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How to Design and Debug a Phase-Locked Loop (PLL) Circuit

By Ray Sun

Introduction

Designing and debugging a *phase-locked loop* (PLL) circuit can be complicated, unless engineers have a deep understanding of PLL theory and a logical development process. This article presents a simplified methodology for PLL design and provides an effective and logical way to debug difficult PLL problems.

Simulation

It is difficult to estimate the specifications of a PLL circuit without simulating it at specific conditions, so simulation should be the first step of the PLL design process. We recommend that engineers use ADIsimPLL™ software to run a simulation based on their system requirements, including *reference frequency*, *step frequency*, *phase noise* (jitter), and *frequency spur* limitations.

Many engineers are confused as to how to choose a reference frequency, but the relationship between the reference frequency and the output frequency step is simple. With an *integer-N* PLL, the output frequency step is equal to the frequency at the input of the *phase-frequency detector* (PFD), which is the reference frequency divided by the reference divider, R. With a *fractional-N* PLL, the output frequency step is equal to the PFD input frequency divided by the *MOD* value, so you can use a higher reference frequency to obtain a smaller frequency step. When deciding whether to use integer-N or fractional-N, the frequency step can be traded for phase noise, with a lower PFD frequency providing better output frequency resolution, but worse phase noise.

As an example, Table 1 shows that if the requirement calls for a fixed-frequency output with a very large frequency step, an integer-N PLL, such as the ADF4106, is preferable due to its better total in-band phase noise. Conversely, if the requirement calls for a small frequency step, a fractional-N PLL, such as the ADF4153, is preferable because its total noise is better than that of the integer-N PLL. Phase noise is an essential PLL specification, but the data sheet cannot specify performance for all possible applications. Thus, simulation followed by testing actual hardware is crucial.

Table 1. Phase Noise Determines Choice of PLL

	Fixed-Frequency Application RF = 1.8 GHz, f_{osc} = 13 MHz, fixed output frequency	GSM1800 Application RF = 1.8 GHz, f_{osc} = 13 MHz, f_{res} = 200 kHz
ADF4106 Integer-N PLL	FOM + 10log f_{pfd} + 20log N = –223 + 10log 13 MHz + 20log 138 = –109 dBc/Hz	FOM + 10log f_{pfd} + 20log N = –223 + 10log 200 kHz + 20log 9000 = –91 dBc/Hz
ADF4153 Fractional-N PLL	FOM + 10log f_{pfd} + 20log N = –220 + 10log 13 MHz + 20log 138 = –106 dBc/Hz	FOM + 10log f_{pfd} + 20log N = –220 + 10log 13 MHz + 20log 138 = –106 dBc/Hz
Result	Integer-N is better	Fractional-N is better

Even when using ADIsimPLL to simulate a PLL circuit under real conditions, the results will probably be insufficient unless model files for the actual reference and voltage-controlled oscillator (VCO) are included. If not, the simulator will use an ideal reference and VCO to do a simulation. The time required to edit a library file for a VCO and reference source will be well worth it when high simulation accuracy is required.

PLLs use a negative-feedback control system similar to that of an amplifier, so the concepts of loop bandwidth and phase margin apply here as well. Generally, the loop bandwidth should be set smaller than one-tenth of the PFD frequency, and the safe range for phase margin is from 45° to 60°. In addition, both simulation and the prototyping on a real board should be performed to confirm that the circuit will meet specifications given the parasitic elements on the PCB layout and the tolerances of resistors and capacitors in the loop filter.

Sometimes suitable values of resistors and capacitors are not readily available, so engineers must determine whether other values will work. A small function called BUILT is hidden in the Tools menu of ADIsimPLL. This function transforms the values of resistors and capacitors to the nearest standard engineering value, allowing the designer to rerun the simulation to verify the new values for phase margin and loop bandwidth.

Registers

ADI PLLs provide many user-configurable options to enable a flexible design environment, but this introduces the challenge of determining the values to store in each register. A convenient solution is to use the evaluation software to set up the register values, even if a PCB isn't connected to the simulator. Afterwards, the setup file can be saved to an .stp file or downloaded to the evaluation board. The simulation results from ADIsimPLL, shown in Figure 1, recommend register values for parameters such as the core current of VCO.

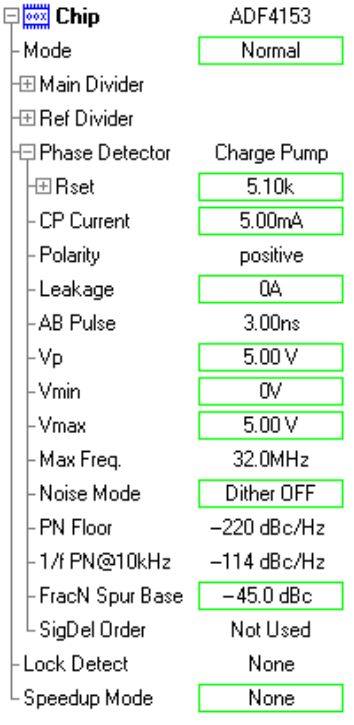

Figure 1. ADIsimPLL simulation software provides recommended values for setup registers.

Schematics and PCB Layout

Several things should be kept in mind when designing the complete PLL circuit. First, it's important to match the impedance at the reference input port of the PLL to minimize reflections. Also, keep the capacitance in parallel with the input port small, as it will decrease the slew rate of the incoming signal and add noise

to the PLL loop. Refer to the input requirements on the PLL data sheet for more detailed information.

Second, separate the analog and digital power supplies to minimize the interference between them. The VCO supply is particularly sensitive, so spurs and noise here can easily couple into the PLL output. Please refer to Powering a Fractional-N Voltage Controlled Oscillator (VCO) with Low Noise LDO Regulators for Reduced Phase Noise (CN-0147) for additional cautions and more detailed information.

Third, the resistors and capacitors used to implement the loop filter should be placed as close as possible to the PLL chip using the values that were recommended by the simulation file. If you have difficulty locking onto a signal after you have changed the values of the loop filter components, please try the original values that were used on the evaluation board.

In terms of the PCB layout, the main principle is to separate the input from the output, making sure that the digital circuitry does not interfere with the analog circuitry. For example, placing the SPI bus too close to the reference input or VCO output will cause spurs on the PLL output when accessing the PLL registers.

From a thermal design perspective, put a thermal ground pad under the PLL chip to ensure that heat flows through the pad to the PCB and heat sink. Designers should calculate all thermal parameters of the PLL chip and PCB when used in extreme environments.

Effective Use of MUXOUT

At the start of the debug phase, it's difficult to determine where to start when the PLL won't lock. As a first step, use MUXOUT to see if each internal function unit is operating properly, as shown in Figure 2. For example, MUXOUT can show the output of the R-counter to indicate that the reference input signal is fine and that the contents of the register were successfully written. MUXOUT can also check to see the detector's lock status and the output of the N-divider in the feedback loop. In this way, the designer can confirm whether the value of each divider, gain, or frequency is correct. This is the fundamental process of debugging a PLL.

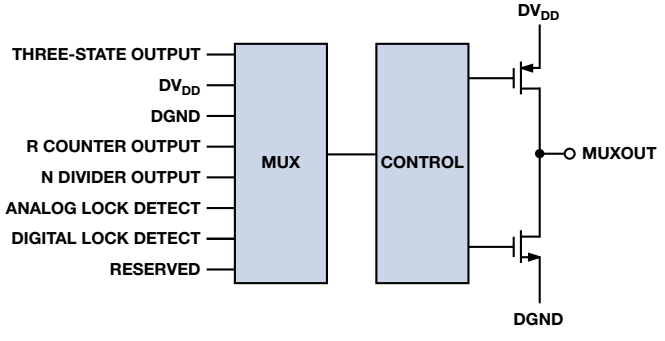

Figure 2. MUXOUT pin aids PLL debugging process.

Time-Domain Analysis

While debugging a PLL, use time-domain analysis to demonstrate that the data written to the registers on the serial peripheral interface (SPI) bus is correct. Even though reads and writes are not done very quickly, make sure that the SPI timing meets specifications and that crosstalk between different lines is minimized.

The timing diagram of the PLL's data sheet should be consulted to determine data setup time, clock speed, pulse width, and other specifications. Be sure to leave enough margin to ensure that the timing requirements are met under all conditions. An oscilloscope should be used to check to see that the clock and data edges are in the right position in the time domain. If clock and data lines are too close, crosstalk can cause energy from the clock to couple to the data line via the PCB traces. This coupling results in a glitch on the data line that occurs on the rising edge of the clock. Therefore, look at these two lines when writing or reading the registers, especially if register errors appear. Make sure that the voltages on the lines are satisfied as shown in Table 2.

Table 2. Logic Inputs

	Minimum	Typical	Maximum	Units
Input High Voltage, V_{INH}	1.5			V
Input Low Voltage, V_{INL}			0.6	V
Input Current, I_{INH}/I_{INL}			±1	μA
Input Capacitance, C_{IN}		3.0		pF

Spectrum Analysis

Issues in the frequency domain are both more frequent and more complex. With a spectrum analyzer, first check to see if the PLL output is locked, as indicated by a stable frequency peak. If not, the tips described above should be followed.

If the PLL is locked, narrow the bandwidth of the spectrum analyzer to determine whether the phase noise is acceptable or not, confirming the test result with the simulation result. Measure the phase noise at several bandwidths, such as 1 kHz, 10 kHz, and 1 MHz, for example.

If the result is not as expected, first review the loop filter design and check the real values of the components on the PCB board. Next, check the reference input to see if its phase noise is the same as the simulation. The simulated phase noise of the PLL should be similar to the real result unless the external conditions are different or the registers were written with the wrong values.

The noise from the power supply should not be ignored, even if a low-noise LDO is used, because both dc-to-dc converters and LDOs look like noise sources. The LDO data sheet usually shows a noise spectrum density that will affect noise-sensitive parts such as PLLs (see Figure 3). Choose a low-noise power source for the PLL, especially to supply the core current of the VCO.

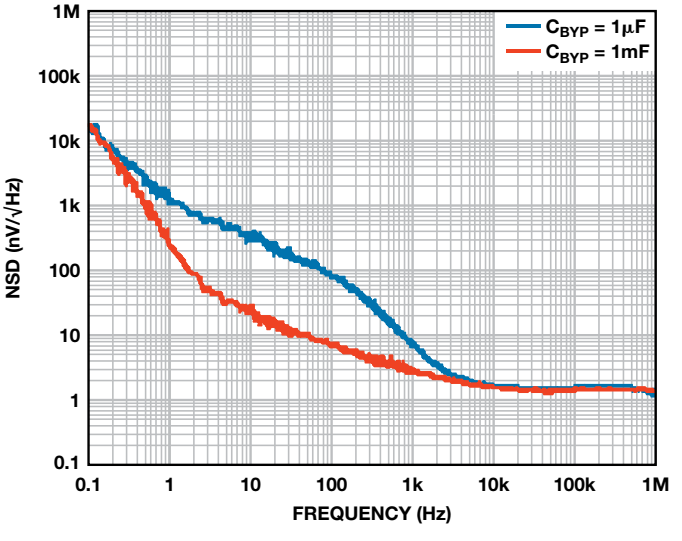

Figure 3. LDO noise spectral density.

Four types of spurs normally appear at the PLL output: PFD or *reference spurs*, *fractional spurs*, *integer boundary spurs*, and *spurs from external sources*, such as the power supply. All PLLs have at least one type of spur, and although they can never be eliminated, we can sometimes improve overall performance by trading spurs of one type or frequency for another.

To avoid reference spurs, check the rising edge of reference signal. An edge that is too fast or too large in amplitude will cause strong harmonics in the frequency domain. Also, carefully check the PCB layout to avoid crosstalk between input and output.

To minimize fractional spurs, dither can be added to push the fractional spurs into the noise floor, but this will increase the noise floor slightly.

Integer boundary spurs are rare, and occur only if the output frequency is too close to an integer multiple of the reference frequency such that the loop filter fails to eliminate it. An easy way to solve this problem is to readjust the reference frequency plan. For example, if a boundary spur occurs at 1100 MHz with an 1100.1-MHz output, a 20-MHz reference input, and a 100-kHz loop filter, changing the reference frequency to 30 MHz will eliminate the spur.

Conclusion

The process of debugging a PLL requires a deep understanding of the PLL, and many problems can be avoided by paying close attention during the design phase. If issues occur during the debugging phase, please follow the suggestions given in this article to analyze the issues one by one and tackle them gradually. For more information, please refer to the wealth of relevant information that can be found on www.analog.com/pll.

References

Curtin, Mike, and Paul O'Brien."Phase-Locked Loops for High-Frequency Receivers and Transmitters—Part 1." *Analog Dialogue*, Volume 33, Number 1, 1999.

Curtin, Mike, and Paul O'Brien. "Phase-Locked Loops for High-Frequency Receivers and Transmitters—Part 2." *Analog Dialogue*, Volume 33, Number 1, 1999.

Curtin, Mike, and Paul O'Brien, "Phase-Locked Loops for High-Frequency Receivers and Transmitters—Part 3." *Analog Dialogue*, Volume 33, Number 1, 1999.

CN0147 Circuit Note. *Powering a Fractional-N Voltage Controlled Oscillator (VCO) with Low Noise LDO Regulators for Reduced Phase Noise*.

Fox, Adrian. "PLL Synthesizers (Ask the Applications Engineer—30)." *Analog Dialogue*, Volume 36, Number 3, 2002.

MT-086 Tutorial. *Fundamentals of Phase-Locked Loops (PLLs)*.

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