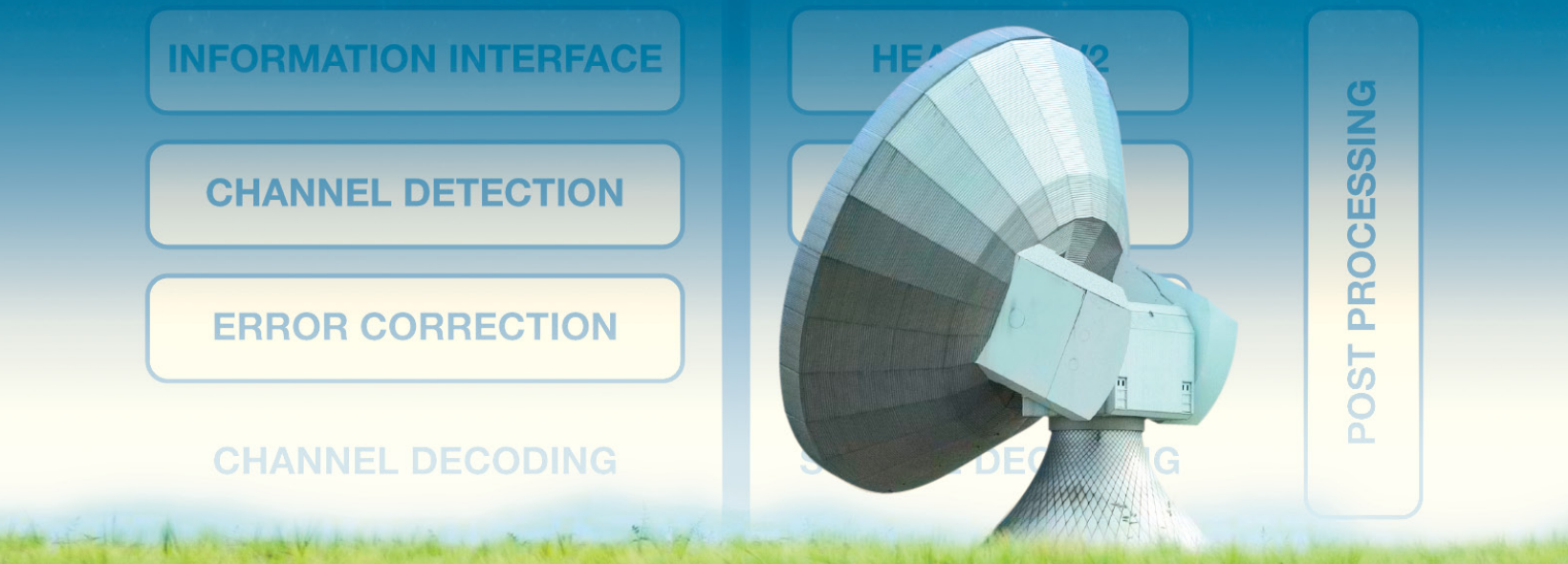
Volume 47, Number 1, 2013

A forum for the exchange of circuits, systems, and software for real-world signal processing

Analog Dialogue

In This Issue



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ANALOG DEVICES

Editor's Notes

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ADI's Engineering University program provides an excellent resource for learning about analog circuitry. The textbook, video lectures, and labs teach analog theory to a high standard, seeding student curiosity; the virtual classroom facilitates international communication, question posing, and remote assistance; and the hardware design platforms inspire students to innovate. (Page 3)

HDMI Made Easy: HDMI-to-VGA and VGA-to-HDMI Converters
The consumer market has adopted High-Definition Multimedia Interface (HDMI) technology in TVs, projectors, and other multimedia devices. This article shows how advanced silicon solutions and smartly implemented software can facilitate HDMI-to-VGA and VGA-to-HDMI converters, which provide engineers familiar with video applications with easy transitions between analog video and digital video. (Page 8)

The Successful Implementation of High-Performance Digital Radio
Broadcast radio is becoming increasingly digital, providing listeners with clearer reception, larger coverage area, higher quality sound, additional content, and increased flexibility in accessing and listening to program material. Using the same bandwidth as analog radio, these improvements could be delivered only by digitizing the content, compressing it, and then broadcasting it digitally. (Page 13)

Modeling Amplifiers as Analog Filters Increases SPICE Simulation Speed
Simulation models for amplifiers are typically implemented with resistors, capacitors, transistors, diodes, dependent and independent sources, and other components—or as s-domain transfer functions. This article presents a method that models amplifiers as second-order analog filters, providing much faster time-domain simulations, especially for higher bandwidth amplifiers. (Page 18)

Convert a Buck Regulator into a Smart LED Driver, Including Dimming
With their long life and low energy consumption, LEDs promise to change the lighting industry, but a key limiter to rapid adoption is the cost of the LEDs themselves. In well-designed systems, LEDs can reliably produce many more lumens per dollar of product cost, so to reduce the total luminaire cost we can drive the LEDs at a much higher current than that at which the device is specified. (Page 23)

Understand How Amplifier Noise Contributes to Total Noise in ADC Signal Chains
ADCs provide optimal performance when the analog inputs are driven to the rated full-scale input voltage, but the maximum available signal often differs from the specified voltage and may need to be adjusted. A useful device for handling this requirement is a variable-gain amplifier (VGA). Understanding how the VGA affects the ADC's performance will help in optimizing performance of the entire signal chain. (Page 27)

A Tribute to Dan Sheingold
On February 1, 2013, Dan Sheingold retired from Analog Devices after 44 years as Editor of *Analog Dialogue*. He won't be leaving the family, though. Dan will assume the mantle of Editor Emeritus, ensuring that he'll continue to be part of the dialogue. Throughout the 47-year history of *Analog Dialogue*, only three people have served as Editor: Ray Stata, Dan Sheingold, and now me, Scott Wayne, Publisher and Managing Editor since 2001. Please join us in offering Dan our best wishes for the future. We'll try to uphold his high quality standards. (Page 30)

Scott Wayne [scott.wayne@analog.com]

PRODUCT INTRODUCTIONS: VOLUME 47, NUMBER 1

Data sheets for all ADI products can be found by entering the part number in the search box at www.analog.com.

January

Regulator, dc-to-dc, 20-V, 6-A, synchronous, step-down..... **ADP2386**
Regulator, dc-to-dc, 36-V, 1-A, synchronous, step-down..... **ADP2442**

February

ADC, sigma-delta, 4-channel, automotive audio systems **ADAU1977**
Amplifier, differential, dual, 4.5-GHz, ultrahigh SFDR **ADL5566**
Amplifier, operational, low-noise, high-speed, low-power **ADA4895-1**
DAC, quad, 12-bit, 180-MSPS, with waveform generator **AD9106**
Decoder, video, 10-bit, SDTV, differential inputs **ADV7182**
Sensors, temperature, digital, 16-bit, ±0.25°C accuracy **ADT7320/ADT7420**
Front-End, analog, 5-electrode ECG systems **ADAS1000-1**
Isolators, digital, 2-channel, with dc-to-dc converter.....**ADuM521x**
Isolators, digital, 4-channel, with switching regulator.....**ADuM447x**
Receiver, HDMI, 165-MHz, low-power..... **ADV7610**
Regulator, 4-A, 20-V, step-down, with low-side driver **ADP2380**

March

Buffer, clock fanout, 1.65-GHz..... **AD9508**
Converter, logarithmic, low-cost, 160-dB range **ADL5303**
Converter, stereo, PDM-to-I^2S or PDM-to-TDM..... **ADAU7002**
DAC, 14-bit, 180-MSPS, with waveform generator **AD9102**
DACs, RF, 11-/14-bit, 5.6-GSPS..... **AD9119/AD9129**
Driver, LED, high-efficiency, eight-string, LCD backlights..... **ADD5201**
Isolators, digital, 2-channel, with dc-to-dc converter.....**ADuM621x**

Analog Dialogue

Analog Dialogue, www.analog.com/analogdialogue, the technical magazine of Analog Devices, discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. Published continuously for 47 years—starting in 1967—it is available in two versions. Monthly editions offer technical articles; timely information including recent application notes, circuit notes, new-product briefs, webinars, and published articles; and a universe of links to important and relevant information on the Analog Devices website, www.analog.com. Printable quarterly issues and ebook versions feature collections of monthly articles. For history buffs, the *Analog Dialogue* archive, www.analog.com/library/analogdialogue/archives.html, includes all regular editions, starting with Volume 1, Number 1 (1967), and three special anniversary issues. To subscribe, please go to www.analog.com/library/analogdialogue/subscribe.html. Your comments are always welcome: Facebook: www.facebook.com/analogdialogue; EngineerZone: ez.analog.com/blogs/analogdialogue; Email: dialogue.editor@analog.com or *Scott Wayne*, Editor [scott.wayne@analog.com].

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Analog Devices' Engineering University—Why YOU Should Attend

By Ryan Fletcher and Scott Wayne

Introduction

Throughout its history, Analog Devices has always been committed to education, as exemplified by its highly trained applications engineers, online EngineerZone community, and extensive portfolio of textbooks, circuit notes, and magazine articles. Unfortunately, in this age of "digital everything," many university students feel that digital electronics seem modern and exciting, while analog electronics appear boring and outmoded. Worse yet, many university curriculums have modeled the interests of their students, boosting their offerings in digital technology, while deemphasizing analog design skills.

The world, however, is analog. Light, sound, temperature, pressure, and acceleration are all analog quantities, so analog sensors, signal conditioning, and data converters will always be required. In addition, although broadcast communications are progressively heading into the digital domain, their RF signals require analog receivers, transmitters, and low-noise amplifiers. Furthermore, as energy efficiency and a "green" Earth become increasingly important, analog power-management techniques are needed more than ever.

Rather than fading out, analog technology is flourishing. In fact, more analog circuitry is found in a state-of-the-art high-definition TV than in a traditional analog TV; cardiac monitoring uses precision analog signal processing to detect small signals buried in noise; modern cell phones require analog power-management circuitry to prolong battery life; automobiles use microelectromechanical systems (MEMS) accelerometers and gyroscopes in electronic stabilization systems; and satellite communications use RF transmitters to broadcast digital signals in an analog realm. So, rather than being quaint, analog technology is now needed more than ever.

Recognizing the gap between the curriculums commonly found at universities and the industry's need for engineers trained in analog circuit design techniques, Analog Devices announced its Engineering University Program in March 2012. Aimed at revolutionizing the way engineering students learn analog circuit design, the program provides engineering students and professors with an affordable portable analog design kit that will enhance their educational experience by allowing them to experiment with advanced technologies, building, and testing real-world analog circuits anytime and anywhere.

In addition to engineering students, the Engineering University Program is ideal for practicing engineers who may be well versed in software development or digital technology but find themselves lacking some of the fundamentals of analog circuit design, technicians who want to improve their understanding of analog circuitry, and hobbyists and inventors who look to acquire new design skills.

The comprehensive program includes a textbook, which features exercises, labs, and homework; software for control, simulation, and analysis; and a design kit that enables hands-on learning. An online community facilitates communication between students, professors, and practicing engineers. As of January 2013, Circuits 1, the first semester course, is available. Future courses, including Circuits 2, Electronics 1, and Electronics 2 are in the works.

Textbook

The well-organized textbook includes homework and labs. Each chapter begins with an introduction and a list of objectives. Worked examples and exercises for the reader are interspersed throughout the text, and section summaries reinforce the lessons learned. The first semester course—Real Analog: Circuits 1—comprises 12 chapters (which are also presented as a series of videos and downloadable lecture slides):

1. **Circuit Analysis Fundamentals**
   This chapter introduces fundamental concepts of voltage, current, and power; basic circuit components including ideal sources and resistors; and analysis techniques such as Kirchhoff's voltage law, Kirchhoff's current law, and Ohm's law. The labs provide the first hint of real-world behavior: resistance varies around the ideal value of a resistor—and the first real-world application of analog circuitry: using a thermistor to measure temperature.

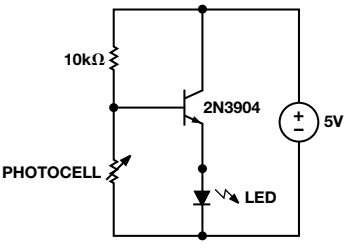

Figure 1. Chapter 1 lab: dawn-to-dusk lighting circuit.

2. **Circuit Reduction**
   This chapter employs the techniques presented in Chapter 1 to analyze series and parallel combinations of resistors and their use as voltage and current dividers. Nonideal sources and nonideal measurement devices provide further examples of real-world behavior.

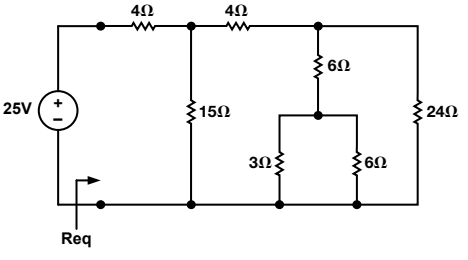

Figure 2. Chapter 2 homework: find the equivalent resistance, Req, and the current provided by the source.

3. **Nodal and Mesh Analysis**
   This chapter introduces the idea of circuit nodes and meshes—including reference nodes, dependent nodes, super nodes, and constrained meshes—offering an easy way to analyze circuit voltages and currents.

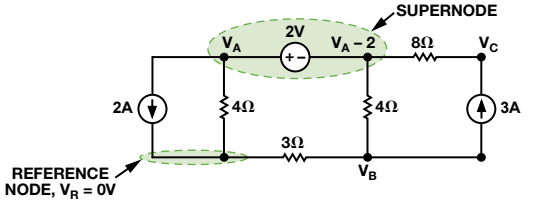

Figure 3. Worked example from Chapter 3 shows reference and super nodes.

4. Systems and Network Theorems

This chapter presents a system-level approach to circuit analysis, representing a conceptual circuit as a real system with inputs and outputs. It defines the mathematical concept of linearity, explains how to use superposition to analyze linear systems, and introduces the powerful Thévenin and Norton theorems that allow complex circuits to be modeled as simpler equivalent circuits. The lab demonstrates how power is transferred from a source to a load and how to match the load to maximize the power transfer.

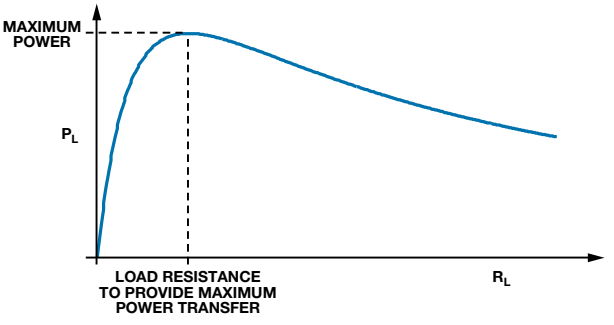

Figure 4. Plot from Chapter 4 shows load power versus load resistance.

5. Operational Amplifiers

This chapter introduces operational amplifiers (op amps), so named because they perform mathematical operations such as addition, integration, and exponentiation. Starting with ideal behavior, which allows easy analysis of inverting, noninverting, and differential circuits, it also explains the effects of real-world behavior, including finite gain, finite input impedance, nonzero output impedance, and nonzero offset voltage. The labs use op amps to improve the temperature measurement system.

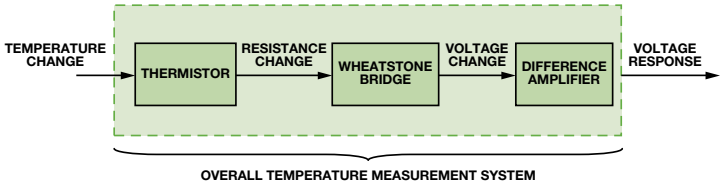

Figure 5. Block diagram from Chapter 5 lab: temperature measurement system design.

6. Energy Storage Elements

This chapter introduces capacitors and inductors, their role as energy storage elements, and their real-world behavior. While all circuits presented in earlier chapters could be analyzed using algebraic equations, these dynamic circuit elements are governed by differential equations. The text defines transient and steady-state responses, and mathematical concepts such as unit-step and decaying exponential functions. The labs generate and observe time-varying waveforms.

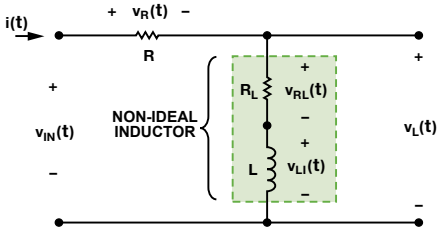

Figure 6. Circuit from Chapter 6 shows nonideal model of an inductor.

7. First-Order Circuits

This chapter features first-order circuits—those that include a single independent energy storage element and are characterized by first-order differential equations. It analyzes the natural response of circuits containing resistors and a single capacitor or inductor, as well as their response to a step change of the input voltage or current. The labs demonstrate how to measure the time constant and step response of active RC circuits.

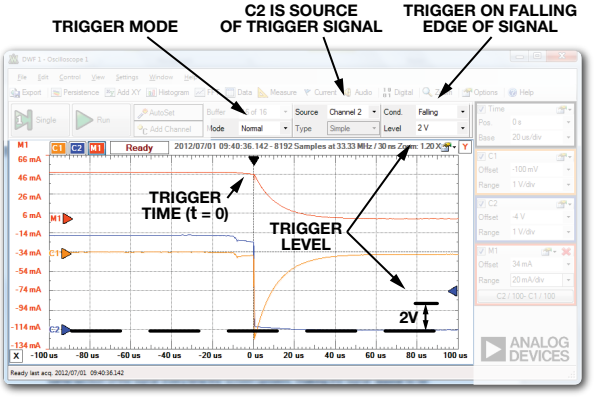

Figure 7. Control panel from Chapter 7 demonstrates trigger time and level.

8. Second-Order Circuits

This chapter expands upon the concepts presented in the previous chapter to analyze second-order circuits— those that include two independent energy storage elements and are characterized by second-order differential equations. While the step response of first-order circuits decays exponentially with time, that of second-order circuits can oscillate, so this chapter introduces the concepts of natural frequency and damping ratio, and relates them to the circuit's rise time, overshoot, and steady-state response. The labs measure the step response of an RLC circuit and analyze why real behavior differs from the ideal calculations.

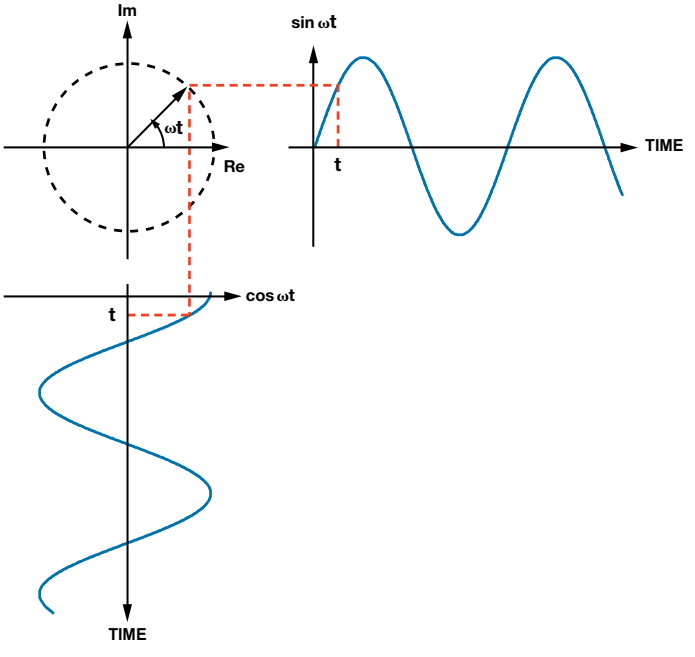

Figure 8. Illustration from Chapter 8 shows relationship between sin ωt, cos ωt, and $e^{j\omega t}$.

9. Introduction to State-Variable Models

This chapter introduces state-variable modeling, which establishes the state of the system using the voltages across the capacitors and the currents through the inductors. The state completely characterizes the system at each instant of time, so knowing the state at any time and the system inputs at all subsequent times allows the output to be determined at any subsequent time. The chapter shows how state-variable modeling enables numerical simulations to determine the system response. The labs in this chapter compare measured results with MATLAB® or Octave simulations.

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_1 \\ 0 & -R/L_2 & 1/L_2 \\ 1/C & -1/C & 0 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} + \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \end{bmatrix} u(t)$$

Figure 9. Matrix algebra from Chapter 9 demonstrates state-variable analysis of third-order circuit.

10. Steady-State Sinusoidal Analysis

This chapter focuses on the steady-state behavior of dynamic systems with sinusoidal inputs, ignoring the system's transient response. It shows how sinusoidal signals can be represented in complex exponential and phasor forms, defines impedance and admittance, and explains how the system's frequency response expresses the relationship between input and output signals. The labs measure the gain and phase of amplifier circuits.

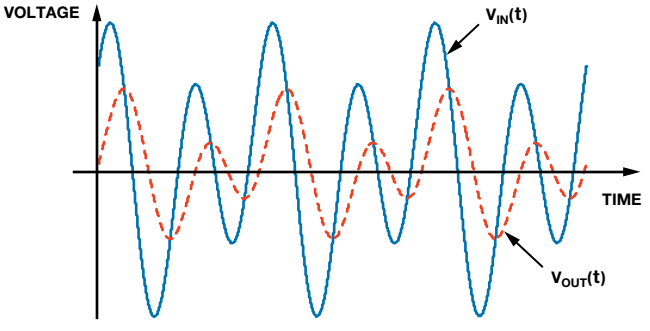

Figure 10. Plot from Chapter 10 shows system response to two-tone input signal.

11. Frequency Response and Filtering

This chapter describes how a system's frequency response can be used as a design and analysis tool and how signals can be represented in terms of their frequency content. It introduces the concepts of signal conditioning, focusing on low-pass and high-pass filters, and shows how Bode plots can illustrate a system's amplitude and phase behavior. The labs include conditioning the output of a MEMS microphone in an audio application and the output of a vibration sensor to measure mechanical stress.

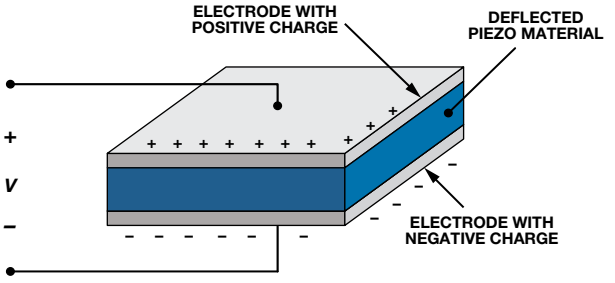

Figure 11. Vibration sensor from Chapter 11 lab project.

12. Steady-State Sinusoidal Power

This chapter covers power transmission using sinusoidal signals and introduces concepts of instantaneous, average, and reactive power. It then shows how to correct the power factor from an inductive load.

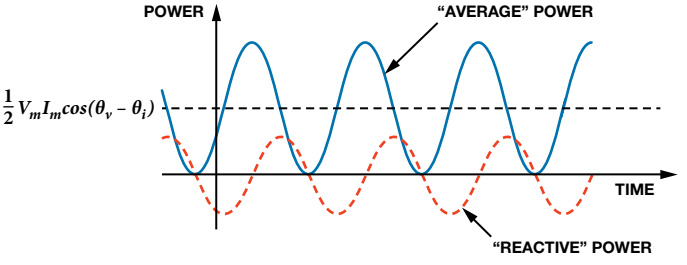

Figure 12. Plot from Chapter 12 shows components of instantaneous power.

Hardware

In addition to theory, the textbook provides practical circuits, discusses nonideal operation, and provides hands-on experience through its lab exercises, but the real fun comes from the design kits. The Analog Discovery™ design kit provides a 2-channel oscilloscope, a 2-channel arbitrary waveform generator, a 16-channel logic analyzer, a 16-channel pattern generator, a 2-channel voltmeter, a network analyzer, and two power supplies, making it a complete, portable, USB-powered analog design lab that enables students to experiment whenever and wherever they have an idea.

Figure 13. Analog Discovery design kit.

The design kit is paired with the Analog Parts Kit, which includes resistors, capacitors, diodes, transistors, sensors, op amps, convertors, regulators, and more—plus, a solderless breadboard, screwdriver, and assorted lead wires.

Figure 14. Analog parts kit.

The design kit uses WaveForms™, a powerful suite of virtual instruments that provides a clean, easy-to-use graphical interface for each instrument, making it simple to acquire, store, analyze, produce, and reuse analog and digital signals.

Figure 15. Waveforms software.

A Student's Perspective

For a student project, I am currently prototyping a device to automatically evaporate condensation from bathroom mirrors. In the process, I have used components of the Analog Devices' Engineering University Program, including the Analog Discovery design kit, WaveForms software, analog parts kit, and online textbook. The vast resources of the program have been invaluable for my project, and other engineering students will surely be thrilled to have it available at their fingertips. Interested students can easily access, transport, and review the program's free online materials in any location. The Analog Discovery hardware design platform allows students to bring the functionality of a traditional lab anywhere. In my case, this versatility triggered an interest in analog circuitry, while encouraging innovation and spur-of-the-moment circuit creation. With these powerful resources at hand, students will be able to explore their deepest curiosities while supplementing the facts learned in their classes.

The online course materials provide some of the program's most intriguing resources. Topics presented in the Real Analog textbook are taught from the perspective of electrical engineers in the workplace, providing excellent insight into subjects traditionally written about by academic writers. Clearly articulated video lectures and PowerPoint slides supplement the written material; and the step-by-step laboratory work develops essential hands-on skills using real-world applications. Freely available online, ADI's Engineering University coursework is perfectly suited to supplement existing course content or as an excellent resource for independent study.

As intellectually stimulating as the online course materials are, perhaps the most useful resources will be those available via the virtual classroom. In this open forum, anyone can pose a question regarding the course materials, technical exercises, or design platforms. The virtual classroom, a key portion of ADI's Engineering University Program, is missing from most other educational packages. Regularly monitored by the professional staff at Analog Devices, this community is designed to encourage collaboration among students. Its ability to foster global communication while offering timely answers to questions will enhance the efficiency of many students.

For me, the most practical portion of the program was the Analog Discovery design kit. With this platform, along with the free WaveForms software, I implemented an oscilloscope, an arbitrary waveform generator, and a power supply—simultaneously from my computer—enabling a quick and easy start to my circuit design. Figure 16 shows a screenshot of the above functions running on my PC. Although I didn't use them for this project, the design kit offers many other features—including a logic analyzer, a pattern generator, static I/O, a voltmeter, and a network analyzer. The device's portability and ease of use will allow students to take creativity and innovation outside of the traditional lab setting and bring it to dormitories, common areas, and even home. Including hardware, which is rarely found as part of an educational package, is an ingenious idea to combine practical design skills with theoretical learning. I highly recommend the optional Analog Parts Kit, which proved to be incredibly useful, providing me with an array of components and saving me the time and hassle of ordering parts.

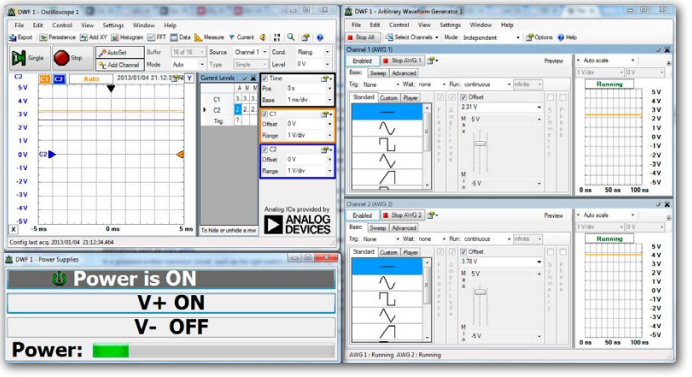

Figure 16. Running an oscilloscope, arbitrary waveform generator, and power supply from a computer.

Figure 17 shows how the Analog Discovery design kit can bring lab functionality anywhere, including the kitchen table. This newfound accessibility to lab tools encourages students to apply their knowledge more creatively, learning debugging techniques and other skills that cannot be taught in lecture. With its portability and ease of use, the design kit provides students with an elegant tool to apply their knowledge.

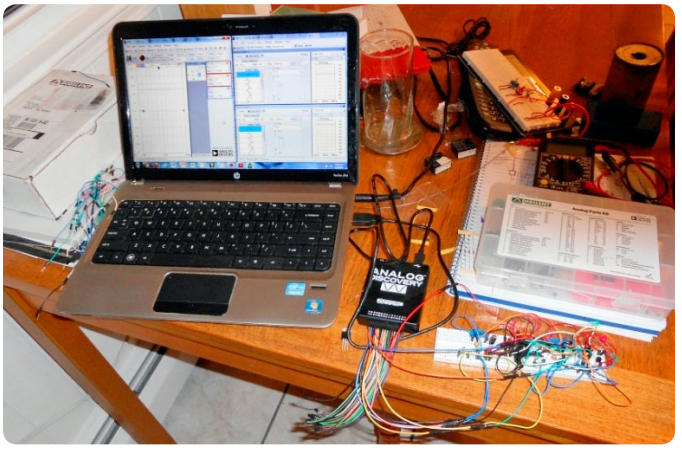

Figure 17. Analog Discovery can bring lab functionality anywhere, including the kitchen table.

As with every educational package, ADI's Engineering University Program has its strengths and weaknesses. Beginning with its strongest points, the courseware is easily accessible and free of charge. Written by individuals who fully understand the content, the online materials leave little room for confusion or misinterpretation. The integration of theory with practical applications provides a near perfect combination of reading and hands-on learning. In addition, the online content blends the components necessary for a complete understanding of the topics, including video lectures, PowerPoint slides, textbook, and reinforcing homework assignments, making the program an exceptional resource for learning about analog circuitry.

The program contains room for improvement, however. The homework lacks sufficient quantity and depth to provide a greater understanding of the material, and the virtual classroom suffers from a lack of participation. The textbook contains some minor formatting inconsistencies and grammatical errors, although these do not hinder the ability of the text to convey information. Lastly, to avoid confusion, Digilent® should include directions to download WaveForms and a manual with the Analog Discovery kit (I had to figure out which software to download and search for documentation that explains the full usage of the package).

For readers who are curious about my project, the device evaporates condensation from bathroom mirrors using a homemade clear thin-film heater, senses the relative humidity and temperature using the AD22100 temperature sensor, and controls the heater with a circuit consisting of comparators and simple transistor logic. Figure 18 shows the breadboard used to prototype and debug the circuit, measure voltages, and simulate the sensor input. ADI's Engineering University Program is proving to be a valuable tool; in the future, I plan to use more of the online course materials to study analog circuitry.

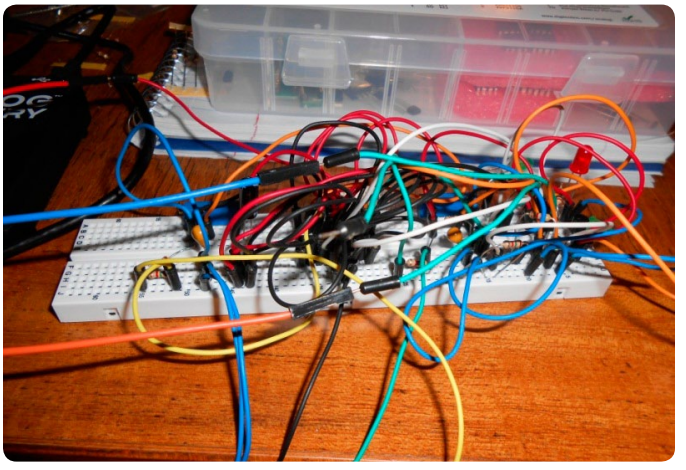

Figure 18. The prototyped circuit on a breadboard.

Conclusion

ADI's Engineering University Program provides an excellent resource for learning about analog circuitry. The textbook, video lectures, and labs teach analog theory to a high standard, seeding student curiosity; the virtual classroom facilitates international communication, question posing, and remote assistance; and the hardware design platforms have superb functionality that inspire students to innovate.

References

Revolutionizing How Engineering Students Learn Analog Circuit Design.

Video about Analog Devices University Program.

Authors

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Scott Wayne [scott.wayne@analog.com] joined Analog Devices as a design engineer in 1978. Before transferring to the *Analog Dialogue* staff, he designed a variety of precision analog-to-digital and digital-to-analog converters using modular, hybrid, and monolithic technologies. Scott holds an SBEE from MIT and continues his education through their edX program. He is the author of several articles and holds two patents. In his free time, Scott enjoys hiking, bicycling, and kayaking.

HDMI Made Easy: HDMI-to-VGA and VGA-to-HDMI Converters

By Witold Kaczurba and Brett Li

The consumer market has adopted High-Definition Multimedia Interface (HDMI®) technology in TVs, projectors, and other multimedia devices, making HDMI a globally recognized interface that will soon be required in all multimedia devices. Already popular in home entertainment, HDMI interfaces are becoming increasingly prevalent in portable devices and automotive infotainment systems.

Implementation of a standardized multimedia interface was driven by a highly competitive consumer market where time to market is a critical factor. In addition to improved market acceptance, using a standard interface greatly improves compatibility between projectors, DVD players, HDTVs, and other equipment produced by various manufacturers.

In some industrial applications, however, the transition from analog video to digital video is taking longer than in the consumer market, and many devices have not yet moved to the new digital approach of sending integrated video, audio, and data. These devices still use analog signaling as their only means of transmitting video, possibly due to specific requirements of a particular market or application. For example, some customers still prefer to use *video graphics array* (VGA) cables for projectors, while others use an *audio/video receiver* (AVR) or media box as a hub, connecting a single HDMI cable to the TV instead of a batch of unaesthetic cables, as outlined in Figure 1.

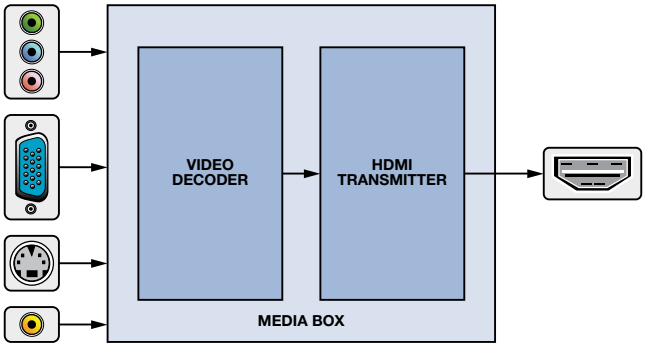

Figure 1. Media box converts analog signal to HDMI.

New adopters may see HDMI as a relatively complicated standard to implement, requiring a validated software driver, interoperability checks, and compliance testing to guarantee proper behavior of one device with various other devices. This might seem a bit overwhelming—as is often the case with new technology.

However, advanced silicon solutions are increasingly available to tackle the problem of implementation complexity, achieving improvement in both analog and digital domains; they include higher performance blocks to equalize poor differential signals and more complex algorithms to reduce software overhead and correct bit errors.

This article shows how advanced silicon solutions and smartly implemented software can facilitate HDMI implementation. Two basic devices—HDMI-to-VGA ("HDMI2VGA") and VGA-to-HDMI ("VGA2HDMI") converters—provide engineers familiar with video applications with an easy way to transition between analog video and digital video.

While HDMI has become a defacto interface for HD video, VGA is still the most common interface on a laptop. This article also shows how to interconnect these video technologies.

Introduction to HDMI Application and Video Standards

HDMI interfaces use *transition-minimized differential signaling* (TMDS) lines to carry video, audio, and data in the form of packets. In addition to these multimedia signals, the interface includes *display data channel* (DDC) signals for exchanging *extended display identification data* (EDID) and for *high-bandwidth digital content protection* (HDCP).

Additionally, HDMI interfaces can be equipped with *consumer electronics control* (CEC), *audio return channel* (ARC), and *home Ethernet channel* (HEC). Since these are not essential to the application described here, they are not discussed in this article.

EDID data comprises a 128-byte long (VESA—Video Equipment Standards Association) or 256-byte long (CEA-861—Consumer Electronics Association) data block that describes the video and (optionally) audio capabilities of the video receiver (*Rx*). EDID is read by a video *source* (player) from the video *sink* over DDC lines using an I^2C protocol. A video source must send the preferred or the best video mode supported and listed in EDID by a video sink. EDID may also contain information about the audio capabilities of the video sink and a list of the supported audio modes and their respective frequencies.

Both VGA and HDMI have the DDC connection to support the communication between source and sink. The first 128 bytes of EDID can be shared between VGA and HDMI. From the experience of the HDMI compliance test (CT) lab at Analog Devices, Inc. (ADI), the first 128 bytes of EDID are more prone to error, since some designers are not familiar with the strict requirements of the HDMI specification, and most articles focus on EDID extension blocks.

Table 1 shows the portion of the first 128 bytes of EDID that is prone to error. The CEA-861 specification can be referenced for details of the CEA extension block design that may follow the first 128 bytes of the EDID.

Table 1. EDID Basic Introduction

Address	Bytes	Description	Comments
00h	8	Header: (00 FF FF FF FF FF FF 00)h	Mandatory fixed block header
08h	10	Vendor and product identification	
08h	2	ID manufacturer name	Three compressed ASCII character code issued by Microsoft®
12h	2	EDID structure version and revision	
12h	1	Version number: 01h	Fixed
13h	1	Revision number: 03h	Fixed
18h	1	Feature support	Features such as power management and color type. Bit 1 should be set to 1.
36h	72	18 byte data blocks	
36h	18	Preferred timing mode	Indicates one supported timing that can produce best quality on-screen images. For most flat panels, the preferred timing mode is the native timing of panel.
48h	18	Detailed timing #2 or display descriptor	Indicates detailed timing, or can be used as display descriptor. Two words should be used as the display descriptor, one as the monitor range limit, and one as the monitor name. Detailed timing block should precede display descriptor block.
5Ah	18	Detailed timing #3 or display descriptor	
6Ch	18	Detailed timing #4 or display descriptor	
7Eh	1	Extension block count N	Number of 128-byte EDID extension blocks to follow.
7Fh	1	Checksum	1-byte sum of all 128 bytes in this EDID block shall equal zero.
80…		Block map or CEA extension	

The timing formats for VGA and HDMI are defined separately by the two standard-setting groups mentioned above: VESA and CEA/EIA. The VESA timing formats can be found in the VESA *Monitor Timing and Coordinate Video Timings Standard*; the HDMI timing formats are defined in *CEA-861*. The VESA timing format covers standards, such as VGA, XGA, SXGA, that are used mainly for PCs and laptops. CEA-861 describes the standards, such as 480p, 576p, 720p, and 1080p, that are used in TV and ED/HD displays. Among the timing formats, only one format, *640 × 480p @ 60 Hz*, is mandatory and common for both VESA and CEA-861 standards. Both PCs and TVs have to support this particular mode, so it is used in this example. Table 2 shows a comparison between commonly supported video standards. Detailed data can be found in the appropriate specifications.

Table 2. Most Popular VESA and CEA-861 Standards (p = progressive, i = interlaced)

VESA (Display Monitor Timing)	CEA-861
640 × 350p @ 85 MHz	720 × 576i @ 50 Hz
640 × 400p @ 85 Hz	720 × 576p @ 50/100 Hz
720 × 400p @ 85 Hz	640 × 480p @ 59.94/60 Hz
640 × 480p @ 60/72/75/85 Hz	720 × 480i @ 59.94/60 Hz
800 × 600p @ 56/60/72/75/85 Hz	720 × 480p @ 59.94/60/119.88/120 Hz
1024 × 768i @ 43 Hz	1280 × 720p @ 50/59.94/60/100/119.88/120 Hz
1024 × 768p @ 60/70/75/85 Hz	1920 × 1080i @ 50/59.94/60/100/200 Hz
1152 × 864p @ 75 Hz	1920 × 1080p @ 59.94/60 Hz
1280 × 960p @ 60/85 Hz	1440 × 480p @ 59.94/60 Hz
1280 × 1024p @ 60/75/85 Hz	1440 × 576p @ 50 Hz
1600×1200p@60/65/70/75/85Hz	720(1440) × 240p @ 59.94/60 Hz
1920 × 1440p @ 60/75 Hz	720(1440) × 288p @ 50 Hz

Brief Introduction to Application and Section Requirements

The key element of HDMI2VGA and VGA2HDMI converters is to ensure that the video source sends a signal conforming to proper video standards. This is done by providing a video source with the appropriate EDID content. Once received, the proper video standard can be converted to the final HDMI or VGA standard.

The functional block diagrams in Figure 2 and Figure 3 outline the respective processes of HDMI2VGA and VGA2HDMI conversion. The HDMI2VGA converter assumes that the HDMI Rx contains an internal EDID.

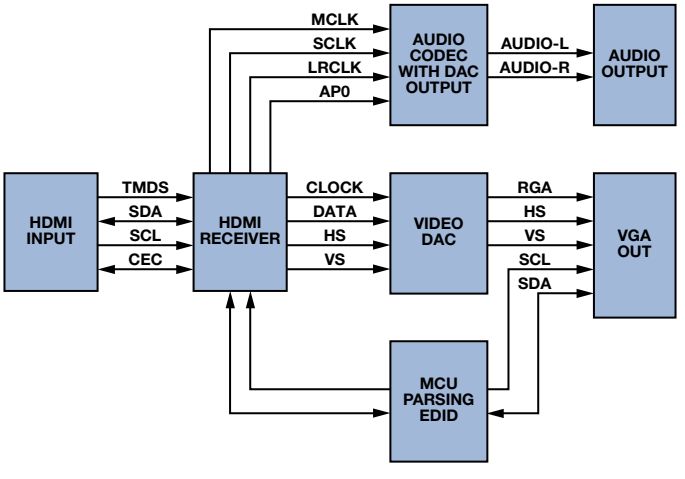

Figure 2. HDMI2VGA converter with audio extraction.

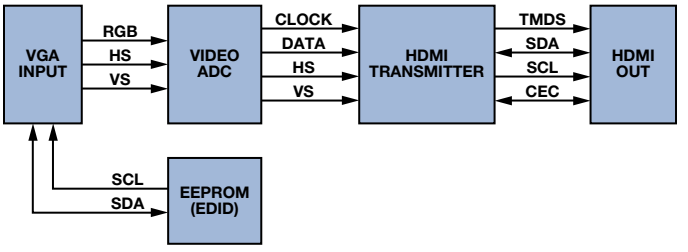

Figure 3. VGA2HDMI converter.

Theory of Operation

VGA2HDMI: a VGA source reads the EDID content from the sink to get the supported timing list using the DDC lines channel, and then the video source starts sending the video stream. The VGA cable has RGB signals and separate horizontal (HSYNC) and vertical (VSYNC) synchronization signals. The downstream VGA ADC locks to HSYNC to reproduce the sampling clock. The incoming sync signals are aligned to the clock by the VGA decoder.

The *data enable* (DE) signal indicates an active region of video. The VGA ADC does not output this signal, which is mandatory for HDMI signal encoding. The logic-high part of DE indicates the active pixels, or the visual part of the video signal. A logic-low on DE indicates the blanking period of the video signal.

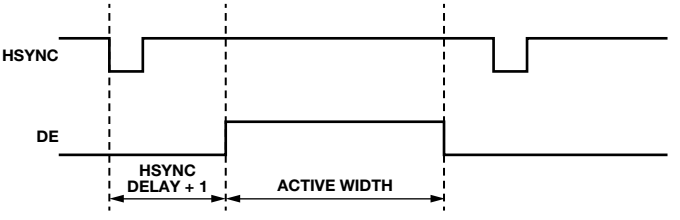

Figure 4. Horizontal DE generation.

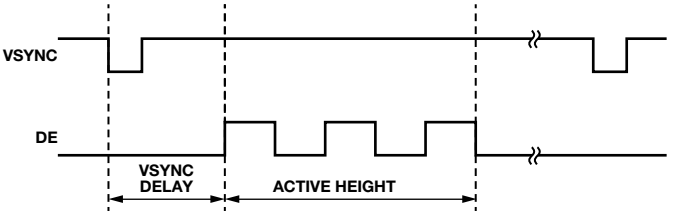

Figure 5. Vertical DE generation.

The DE signal is critical in order to produce a valid HDMI stream. The lack of a DE signal can be compensated for by the HDMI transmitter (Tx), which has the capability to regenerate DE. Modern HDMI transmitters can generate a DE signal from the HSYNC and VSYNC inputs using a few parameter settings, such as HSYNC delay, VSYNC delay, active width, and active height—as shown in Figure 4 and Figure 5—ensuring compatibility for HDMI signal transmission.

The HSYNC delay defines the number of pixels from the HSYNC leading edge to the DE leading edge. The VSYNC delay is the number of HSYNC pulses between the leading edge of VSYNC and DE. Active width indicates the number of active horizontal pixels, and active height is the number of lines of active video. The DE generation function can also be useful for display functions such as centering the active video area in the middle of the screen.

Display position adjustment is mandatory for VGA inputs. The first and last pixel of the digitized analog input signal must not coincide with or be close to any HSYNC or VSYNC pulses. The period when the DE signal is low (such as the vertical or horizontal blanking interval) is used for transmitting additional HDMI data and audio packets and, therefore, cannot be violated. The ADC sampling phase can cause this kind of misalignment. An active region misalignment may be suggested by a black stripe on the visual area of the screen. For a composite video broadcast signal (CVBS), this phenomenon can be corrected by overscanning by 5% to 10%.

VGA is designed to display the whole active region without eliminating any area. The picture is not overscanned, so the display position adjustment is important for VGA to HDMI conversion. In a best-case scenario, the black stripe can be automatically recognized, and the image can be automatically adjusted to the middle of the final screen—or manually adjusted according to the readback information. If the VGA ADC is connected to the back-end scaler, the active video can be properly realigned to the whole visible area.

However, using the scaler to fix an active video region misalignment increases the cost of the design and the associated risks. With a scaler and a video pattern, for example, a black area surrounding a small white box inside the active region could be recognized as a useless bar and removed. The white box would become a pure white background when the black area was removed. On the other hand, an image with half white and half black would result in distortion. Some prevention mechanism must be integrated to prevent this kind of incorrect detection.

Once the HDMI Tx locks and regenerates the DE signal, it starts sending the video stream to an HDMI sink, such as a TV. In the meantime, the on-board audio components, such as the audio codec, can also send the audio stream by I^2S, S/PDIF, or DSD to the HDMI Tx. One of the advantages of HDMI is that it can send video and audio at the same time.

When a VGA2HDMI conversion board powers up and the source and sink are connected, the MCU should read back the EDID content of the HDMI sink via the HDMI Tx DDC lines. The MCU should copy the first 128 bytes of EDID to the EEPROM for the VGA DDC channel with minor modification since the VGA DDC channel does not usually support the CEA extension used for HDMI. Table 3 provides a list of required modifications.

Table 3. List of Modifications Needed for a VGA2HDMI Converter

Modification	Reason
Change EDID 0x14[7] from 1 to 0	Indicates analog VGA input
Modify established timing, standard timing, preferred timing, and detailed timing	Timing beyond the maximum supported by the VGA converter and HDMI Tx must be changed to maximum timing or below
Set 0x7E to 00	No EDID extension block
Change 0x7F	Checksum has to be recalculated based on above changes

HDMI2VGA: the HDMI2VGA converter has to first provide proper EDID content to the HDMI source prior to receiving the desired 640 × 480p signal—or other standard commonly supported by the video source and display. An HDMI Rx usually stores the EDID content internally, handles the *hot plug detect* line (indicating that a display is connected), and receives, decodes, and interprets incoming video and audio streams.

Since the HDMI stream combines audio, video, and data, the HDMI Rx must also allow readback of auxiliary information such as color space, video standards, and audio mode. Most HDMI receivers adapt to the received stream, automatically converting any color space (YCbCr 4:4:4, YCbCr 4:2:2, RGB 4:4:4) to the RGB 4:4:4 color space required by the video DAC. Automatic *color space conversion* (CSC) ensures that the correct color space is sent to a backend device.

Once an incoming HDMI stream is processed and decoded to the desired standard, it is output via pixel bus lines to video DACs and audio codecs. The video DACs usually have RGB pixel bus and clock inputs without sync signals. HSYNC and VSYNC signals can be output through the buffer to the VGA output and finally to the monitor or other display.

An HDMI audio stream can carry various standards, such as L-PCM, DSD, DST, DTS, *high-bit-rate audio,* AC3, and other compressed bit streams. Most HDMI receivers do not have a problem extracting any audio standard, but the further processing might. Depending on the backend device, it may be preferable to use a simple standard rather than a complex one to allow easy conversion to the analog output for speakers. HDMI specifications ensure that all devices support at least 32 kHz, 44.1 kHz, and 48 kHz LPCM.

It is, thus, important to produce EDID that matches both the audio capability of the HDMI2VGA converter that extracts the audio and the original capabilities of the VGA display. This can be done by using a simple algorithm that retrieves EDID content from the VGA display via DDC lines. The readback data should be parsed and verified to ensure that the monitor does not allow higher frequencies than those supported by the HDMI Rx or video DAC (refer to Table 4). An EDID image can be extended with an additional CEA block that lists audio capabilities to reflect that the HDMI2VGA converter supports audio only in its linear PCM standard. The prepared EDID data containing all the blocks can, therefore, be provided to the HDMI source. The HDMI source should reread EDID from the converter after pulsing the *hot plug detect* line (part of the HDMI cabling).

A simple microcontroller or CPU can be used to control the whole circuit by reading the VGA EDID and programming the HDMI Rx and audio DAC/codec. Control of the video DACs is usually not required, as they do not feature control ports such as I^2C or SPI.

Table 4. List of Modifications Needed for an HDMI2VGA Converter

Modification	Reason
Change 0x14[7] from 0 to 1	Indicates digital input
Check standard timing information and modify if necessary (bytes 0x26 to 0x35)	Timing beyond the maximum supported by the converter and HDMI Rx must be changed to maximum timing or below
Check DTD (detailed timing descriptors) (bytes 0x36 to 0x47)	Timing beyond the maximum supported by the converter and HDMI Rx must be changed to maximum timing or below (to 640 × 480p, for example)
Set 0x7E to 1	One additional block must be added at end of EDID
Change 0x7F	Checksum must be recalculated from bytes 0 to 0x7E
Add extra CEA-861 block	
0x80 to 0xFF describing audio	Add CEA-861 block to indicate audio converter capabilities

Content Protection Considerations

Since typical analog VGA does not provide content protection, standalone converters should not allow for the decryption of content-protected data that would enable the end user to access raw digital data. On the other hand, if the circuit is integral to the

larger device, it can be used as long as it does not allow the user to access an unencrypted video stream.

Example Circuitry

An example VGA-to-HDMI board can use the AD9983A high-performance 8-bit display interface, which supports up to UXGA timing and RGB/YPbPr inputs, and the ADV7513 high-performance 165-MHz HDMI transmitter, which supports a 24-bit TTL input, 3D video, and variable input formats. It is quick and convenient to build up a VGA2HDMI converter using these devices. The ADV7513 also features a built-in DE generation block, so no external FPGA is required to generate the missing DE signal. The ADV7513 also has an embedded EDID processing block and can automatically read back the EDID information from the HDMI Rx or be forced to read back manually.

Similarly, building an HDMI2VGA converter is not overly complicated; a highly integrated video path can be built with the ADV7611 low-power, 165-MHz HDMI receiver and the ADV7125 triple, 8-bit, 330-MHz video DAC. The Rx comes with built-in internal EDID, circuitry for handling *hot plug assert,* an automatic CSC that can output RGB 4:4:4, regardless of the received color space, and a component processing block that allows for brightness and contrast adjustment, as well as sync signal realignment. An SSM2604 low-power audio codec allows the stereo I²S stream to be decoded and output with an arbitrary volume through the DAC. The audio codec does not require an external crystal, as the clock source can be taken from the ADV7611 MCLK line, and only a couple of writes are required for configuration.

A simple MCU, such as the ADuC7020 precision analog microcontroller with a built-in oscillator, can control the whole system, including EDID handling, color enhancement, and a simple user interface with buttons, sliders, and knobs.

Figure 6 and Figure 7 provide example schematics for the video digitizer (AD9983A) and HDMI Tx (ADV7513) essential for a VGA2HDMI converter. MCU circuitry is not included.

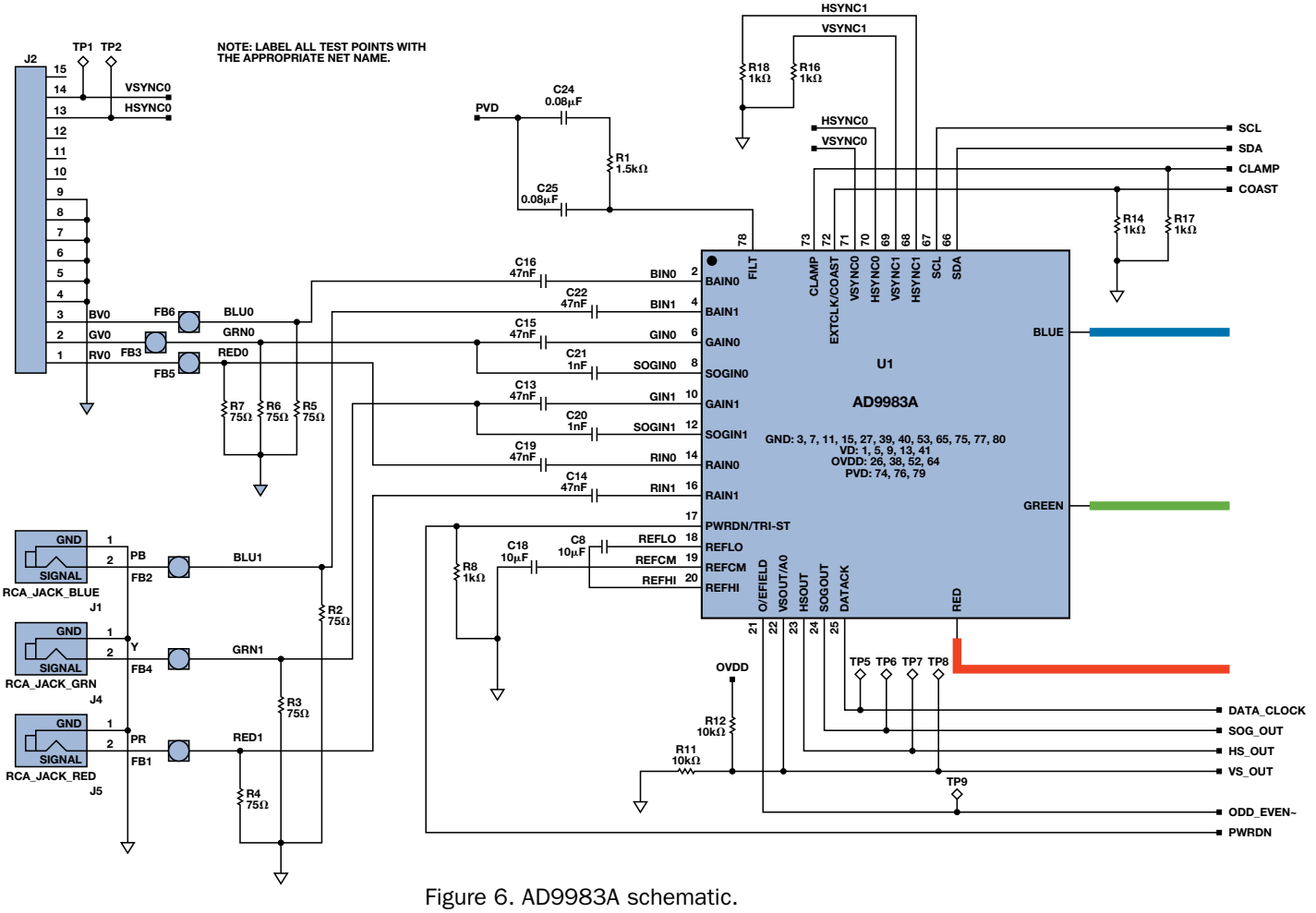

Figure 6. AD9983A schematic.

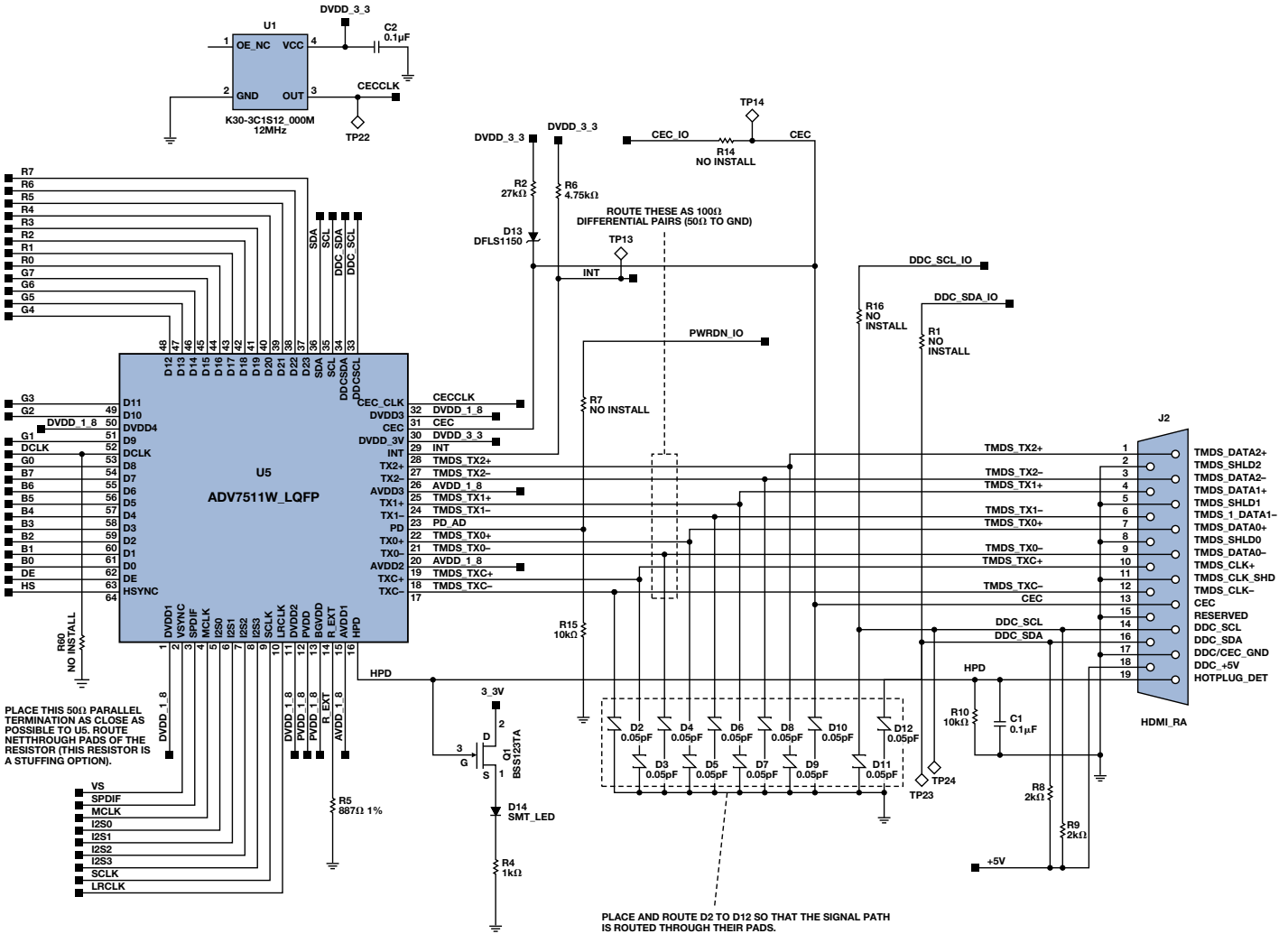

Figure 7. ADV7513 schematic.

Conclusion

Analog Devices audio, video, and microcontroller components can implement highly integrated HDMI2VGA or VGA2HDMI converters that can be powered with the small amount of power provided by a USB connector.

Both converters show that applications using HDMI technology are easy to apply with ADI components. HDMI system complexity increases for devices that are supposed to work in an HDMI repeater configuration, as this requires handling the HDCP protocol along with the whole HDMI tree. Neither converter uses an HDMI repeater configuration.

Applications such as video receivers (displays), video generators (sources), and video converters require a relatively small software stack and, therefore, can be implemented in a fast and easy way. For more details and schematics, refer to ADI's EngineerZone Web pages.

References

A DTV Profile for Uncompressed High Speed Digital Interfaces (CEA-861-E).

Display Monitor Timing (DMT), Coordinated Video Timings (CVT), and Enhanced Extended Display Identification Data (E-EDID) standards are available from VESA.

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The Successful Implementation of High-Performance Digital Radio

By T.V.B. Subrahmanyam and Mohammed Chalil

Evolution of Digital Radio

Amplitude modulation (AM) was the dominant form of radio broadcasting during the first 80 years of the 20th century, but channel fading, distortion, and noise led to poor reception quality. These problems were reduced to some extent with the introduction of frequency modulation (FM), which could also provide stereo transmission and CD-quality audio, but analog radio was still not devoid of channel imperfection effects and limited coverage area. During 2003, two commercial start-ups, XM and Sirius (these merged and became SiriusXM™), introduced the huge footprint of subscription-based digital satellite radio in the United States, with a revenue model similar to that of Pay-TV channels. Around the same time, WorldSpace Radio started satellite broadcasts for Asia and Africa.

The Satellite Digital Audio Radio Services (SDARS) enabled mobile car audio listeners to tune into the same radio station anywhere within the satellite's coverage map, limited only by intermittent blockage of satellite signal due to buildings, foliage, and tunnels. XM satellite radio took the lead in circumventing the blockage problem by installing terrestrial repeaters, which transmit the same satellite audio in dense urban areas and create a hybrid architecture of satellite and terrestrial broadcasts.

Around the same time the *traditional* terrestrial broadcasters also charted a digital course—for two reasons. First, they perceived that their life span on the *analog* concourse had to be quite short, as the world migrates to the higher quality *digital* runway. Second, the frequency spectrum is getting scarce, so additional content within the same bandwidth could be delivered only by digitizing and compressing the old and new content, packaging it, and then broadcasting it. Thus, the world started migrating from analog to digital radio. These techniques for radio broadcast had the advantages of clearer reception, larger coverage area, and ability to pack more content and information within the existing bandwidth of an available analog radio channel—as well as offering users increased control flexibility in accessing and listening to program material (Figure 1).

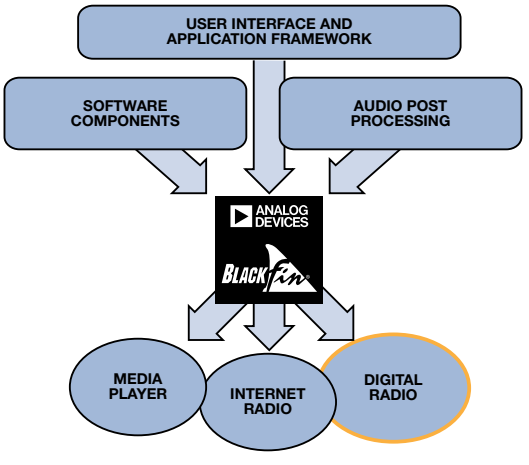

Figure 1. Digital radio on a convergence processor.

Digital Radio Development Example: India

In terrestrial broadcasting, there are two open standards—Digital Multimedia Broadcasting (DMB) and Digital Radio Mondiale™ (DRM)—and HD Radio,™ a proprietary standard from iBiquity (the only standard approved by the FCC for AM/FM audio broadcasting within the United States). DMB specifies several formats for digital *audio broadcasting*, including DAB, DAB+, and T-DMB, which use VHF Band III and L-band. DRM uses DRM30, which operates from 150 kHz to 30 MHz, and DRM+ in VHF Bands I, II, and III.

Useful propagation in the VHF bands is essentially limited to line-of-sight in small geographic regions. Propagation in short wave, on the other hand, can go almost anywhere in the world due to multiple reflections in the ionosphere. For countries that are densely populated and have small geographic regions, DMB transmitting in VHF Band III and L-Band functions very efficiently. For countries that have large geographic areas, transmissions in medium and short wave provide effective coverage. For this reason, after a few years of trials of DAB and DRM, India decided to adopt DRM.

During 2007, All India Radio (AIR), Asia-Pacific Broadcasting Union (ABU), and the DRM Consortium conducted the first field trial for DRM in New Delhi. The experimental trial was conducted over three days with three transmitters, with measurements of various parameters. Besides these tests in New Delhi, AIR also did these measurements at long distances. It became clear that DRM had the advantage of serving a larger population with a limited number of transmitters. In addition, the increasing need for energy conservation raises power saving considerations to paramount importance. DRM's 50% greater power efficiency plays a vital role in supporting the ecology and a "greener" Earth.

Digital Radio Receivers and DSP

The physical world is *analog*, yet scientists and engineers find it easier to do a lot of computation and symbol manipulation in the *digital* domain. Thanks to sampling theory, signal processing, and available data converters, the way is smoothly paved for engineers to design, implement, and test complex *digital signal-processing* (DSP) systems using *analog-to-digital* converters (ADCs) and *digital signal processors* with programmable cores.

Development of powerful and efficient DSPs—along with advancements in information and communication theory—enabled the convergence of media technology and communications. Digital radio owes its existence to these technological advances.

Digital radio receivers were initially designed as lab prototypes and then moved to pilot production. Like most technologies, the first generation products are generally assembled using discrete components. As the market size and competition increase, manufacturers find that markets can be further expanded by bringing down the price of the finished product. The prospect of higher volume attracts semiconductor manufacturers to invest in integrating more of these discrete components to bring down the cost. With time, the shrinking silicon geometries lead to further cost reductions and improvements in the product's capability. Such has been the continuing evolution in many products, including FM radios and mobile phones.

Signal Processing in Digital Radio

A typical digital communication system (Figure 2) converts the analog signal into digital, compresses it, adds error-correction code, and packs several signals to make best use of the channel capacity. To transmit RF signals (which exist in the "real" world of analog energy), the digital signal is converted into analog and modulated on a carrier frequency for transmission. At the receiver, the reverse process takes place, starting with demodulating the carrier frequency. The signal is then converted to digital, checked for errors, and decompressed. The baseband audio signal is converted to analog, ultimately producing acoustic sounds.

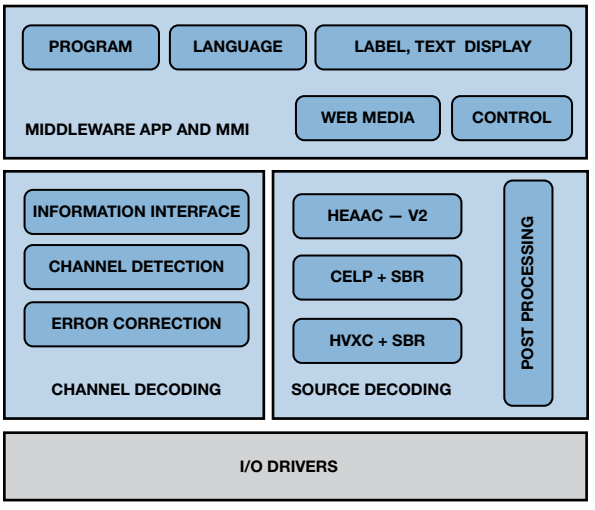

Figure 2. Software architecture of digital radio.

Signal processing algorithms in a digital radio receiver can be classified into the following categories:

- Channel decoding
- Source decoding
- Audio post processing
- Middleware
- User interface (MMI)

In digital radio, the *source coding* and *channel coding* can respectively be mapped to an efficient audio *codec* (coder-decoder) and *error control* system components. Practically, error control can be performed better if the codec is designed for error resilience.

An ideal channel coder should be resilient to transmission errors. An ideal source coder should compress the message to the highest information content (Shannon entropy), but highly compressed messages would lead to very high audio distortion if the input stream contains errors. Thus, effective source coding should also ensure that the decoder can detect the errors in the stream and conceal their impact so that overall audio quality is not degraded.

DRM applies relevant technological innovations in source coding and channel coding to deliver a better audio experience. The DRM audio source coding algorithm that is selected ensures:

- Efficient audio coding—higher audio quality with lower bit rate.
- Better error resilience—aesthetic degradation under transmission errors.

Efficient Audio Source Coding

Motion Picture Experts Group (MPEG) technology can be considered as the conduit and framework for effective collaboration of academic, industry, and technology forums. Success of such collaborative audio-specific efforts as MPEG Layer II, MP3, and AAC (advanced audio coding) for broadcasting and storage/distribution, respectively, has encouraged the industry to engage in further research initiatives. MP3 continues to be the most popular 'unofficial' format for web distribution and storage, but simpler licensing norms—and Apple's decision to adopt AAC as the media form for the iPod—have helped AAC to get more industry attention than MP3.

Let us consider AAC from the MPEG community to understand some of the important technologies involved in source coding. *Psycho acoustic model* (Figure 3) and *time-domain alias cancellation* (TDAC) can be considered as two initial breakthrough innovations in wideband audio source coding.

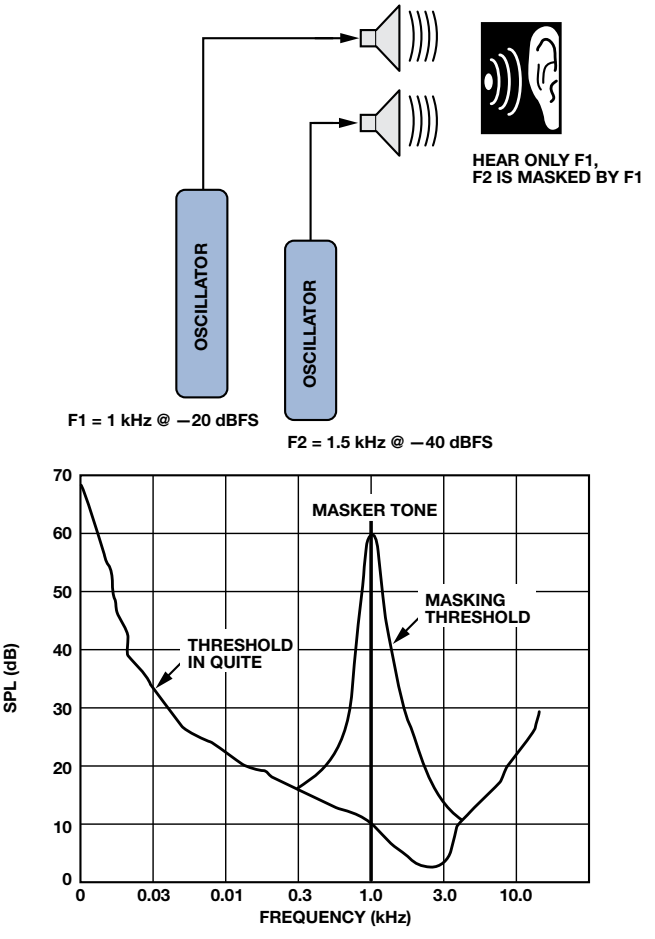

Figure 3. Understanding psycho-acoustic tonal masking.

Spectral band replication (SBR, Figure 4) and *spatial audio coding* or *binaural cue coding* techniques from industry and academia can be considered as the next two game-changing innovations. These two key breakthrough innovations further enhanced AAC technologies to give scalable coding performance, which resulted in standardization of HE-AAC v2 and MPEG *surround*—which received overwhelming responses from the industry. Industry-driven standards, like Dolby,® AC3, and WMA,® also took similar steps to leverage similar technological innovations for their latest media coding.

The *spectral band replacement* (SBR) tool doubles the decoded sample rate relative to the AAC-LC sample rate. The *parametric stereo* (PS) tool decodes stereo from a monophonic LC stream.

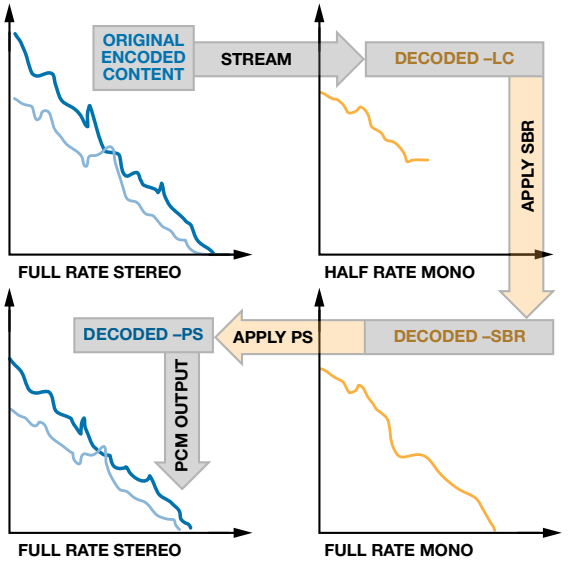

Figure 4. AAC-LR, SBR, and PS in audio decoding.

Like any other improvement initiatives, measurement technologies also played their role in audio quality improvement initiatives. Audio quality evaluation tools and standards, like *perceptual evaluation of audio quality* (PEAQ) and *multi-stimulus with hidden reference and anchor* (MUSHRA), aided faster evaluation of technological experiments.

Graceful Degradation/Error Resilience

In general, higher compression will lead to more audio artifacts from a given level of stream errors. For example, the MPEG Layer II stream is more robust to stream errors than AAC streams. A single-bit error in spectral data part of Layer II wouldn't make any annoying artifacts, as the spectral value maximum is decided by the bit-allocation value. However, in the case of AAC, the same single-bit error would cause the Huffman decoder to fail and apply frame error concealment; repetitive frame errors will mute the audio until the error rate is reduced to minimum. This long silence prevents the system from guaranteeing graceful degradation.

Error Resilience (ER) AAC coding guarantees graceful degradation from bit-stream errors with the help of these additional tools:

- HCR (*Huffman codeword reordering*): error propagation within spectral data is prevented by dividing the spectral data into fixed size segments. HCR places the most important data at the start of each segment.
- VCB11 (*virtual codebooks for codebook 11*): detects serious errors within spectral data with the help of special code word mapping.
- RVLC (*reversible variable length coding*): avoids error propagation in scale factor data.

The ER-AAC features, together with UEP, will provide adequate error resilience characteristics for DRM.

DRM Specification

Digital Radio Mondiale (DRM) is an open standard from European Telecommunication Standards Institute (ETSI) for digital narrow-band audio for short and medium-wave broadcasting. Although DRM supports bandwidths of 4.5 kHz, 5 kHz, 9 kHz, 10 kHz, 18 kHz, and 20 kHz within four modes of transmission and reception, bandwidth and bit rate must be limited to 10 kHz and 24 kbps, respectively, if compatibility with existing AM standards is desired.

Table 1. DRM bit-rate-bandwidth.

Bandwidth at 30 MHz	Bandwidth (kHz)	Bit Rate (kbps)
Nominal BW	9 to 10	8 to 20
Half BW	4.5 to 5	2 or 4
Double BW	18 to 20	20 to 80

This requirement demanded the use of highly efficient audio coding: Meltzer-Moser MPEG-4 HE-AAC v2 (International Standardization Organization/International Electrotechnical Commission—ISO/IEC) was a good choice, but the robustness against channel fading made an error-resilient version of HE-AAC v2 (Martin Wolters, 2003) the *best* choice.

Table 2. Different codecs supported by DRM.

Bit Rate (kbps)	20 to 80	8 to 20	2 to 4
Codec	AAC	CELP	8 to 20
Audio Rate	12, 24, or 48	8 to 16	2 or 4
SBR	Yes	Yes	Yes
PS	Yes	—	—
Double BW	Yes	Yes	Yes

Besides AAC, the DRM standard defines the harmonic vector excitation coding (HVXC) and code-excited linear prediction (CELP) codecs to be used for transmitting speech. Streaming raw data for image slideshows, HTML pages, and the like is also allowed by the DRM standard.

DRM Architecture

A DRM system comprises three main transmission paths: main service channel (MSC), service description channel (SDC), and fast-access channel (FAC). The FAC carries the orthogonal frequency-division multiplexed (OFDM) signal properties and the SDC/MSC configuration—and is limited to 72 bits/frame. The SDC contains the information needed for MSC decoding, such as the multiplex frame structure—and other information.

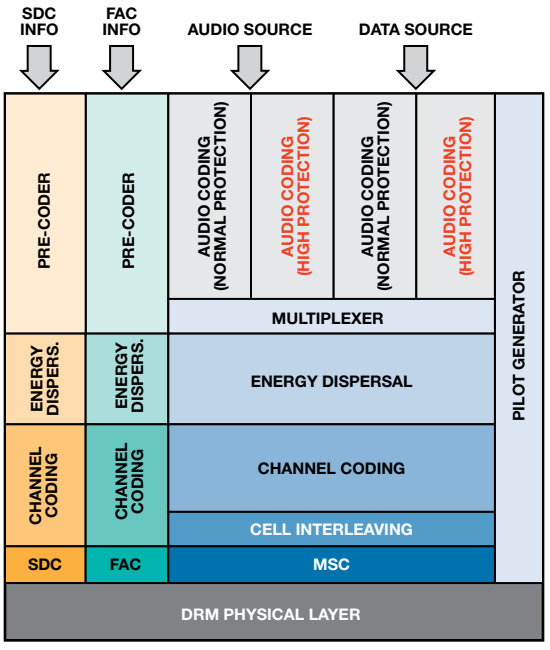

Figure 5. Multiplexing and channel coding in DRM.

The MSC encodes the frame generated by the multiplexer. One can choose between standard mapping, symmetrical hierarchical, or mixed hierarchical mapping. The MSC uses unequal error protection (UEP, Figure 6), in which the multiplex frame is split into two parts with different levels of protection: higher- and lower-protected data parts.

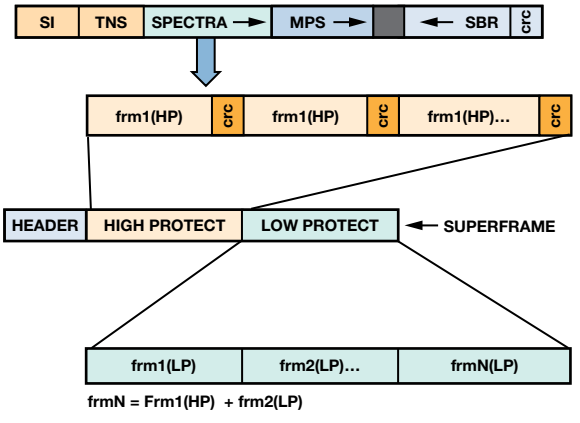

Figure 6. Unequal error protection in DRM.

Digital Radio with Blackfin

The Blackfin® processor (Figure 7) is an excellent fit for operations requiring both digital signal processing and a microcontroller function. The ADSP-BF5xx family is particularly suitable for these applications and also offers a variety of peripherals. Availability of hardware and software development tools, several software components from third parties, and reference designs make it an ideal platform for multifeatured products. Multiple generations of products, availability of mature software IP from dependable sources, reliable support from ADI, and the large portfolio of available high-performance analog integrated circuits support the quality of a designer's end products.

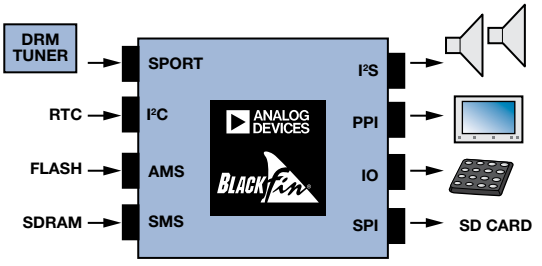

Figure 7. Blackfin processor based digital radio.

Blackfin processor based digital radios, Internet radios, and multi-featured products can be created using the existing ecosystem that ADI created for these products.

In addition to creating the required ecosystem and sourcing the various software modules, ADI also created its own decoder libraries for digital radio. One such key component is an HE-AAC v2 decoder, which optimizes the performance available from the large number of required MIPS.

Architecture of HE-AAC V2 Decoder

HE-AAC v2 decoder components (Figure 8) combine to form the DRM source decoder. The MPEG-4 HE-AAC v2 decoder (which can support ETSI DAB and DRM standards) combines advanced audio coding (AAC), spectral band replication (SBR), and parametric stereo (PS). The decoder is backward compatible with AAC-LC.

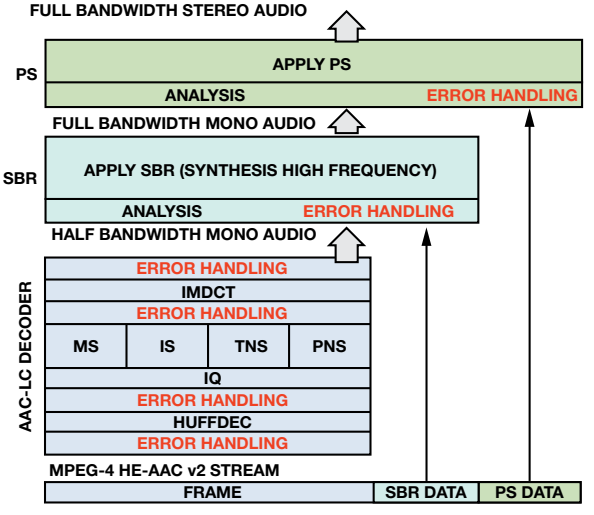

Figure 8. MPEG-4 HE-AAC v2 decoder.

Key features include:

- MPEG-4 ER-AAC scalable decoder that can handle 960 samples per frame
- AAC-LC/HE-AAC v1/v2/DRM/DAB support
- Error concealment support
- DRC support
- Highly optimized for memory and MIPS
- Validates against a complete set of ISO/DAB/DMB and ETSI vectors.

Table 3. MPEG-4 HE-AAC v2 decoder performance.

Memory in kB	Code	Table	Data	MIPS
DAB	115	61	182	8 to 20
DRM	115	62	182	2 or 4

The decoder implements all required audio coding tools specified by the standard, including:

- Higher frequency resolution and coding efficiency due to MDCT/TDAC
- Adaptive block switching reduces pre-echo
- Nonlinear quantization
- Huffman coding
- Use of Kaiser-Bessel derived window function to eliminate spectral leakage.
- Variable frame-size improves bit-allocation
- IS/MS stereo/TNS and PNS tools
- Spectral band replication (SBR)
- Parametric stereo (PS)

Digital Radio Test Results

A set of typical test results appears in Table 4.

Table 4. Digital radio test results.

Parameter	Results
Sensitivity	40 dB
Half BW	5 dB better than MRR
Inter-Modulation	>57 dB
Dynamic Range	25 dB more than MRR
Adj. Ch. Suppression	MRR +5 dB at ±10 kHz
Reception Freq. Offset	400 Hz better than MRR
Operating Voltage	6.5 V to 12 V

Conclusion

Analog Devices, Inc., (ADI) was an early participant in implementing digital radio and performing field trials of the reference design. A Blackfin processor-based DRM radio was one of the first designs that met all *minimum receiver requirements* (MRR) stipulated by the DRM standards. That success can be attributed to excellent teamwork, in which ADI managed and partnered with BBC in the UK, Dolby (erstwhile Coding Technologies) in the US, and Deutsche Welle and AFG Engineering in Germany. The technology and reference design was then adopted by apparatus manufacturers to engineer and make products.

Now, additional companies are using this design for making digital radios in India and other countries. The ADI Blackfin processor has the right combination of DSP and microcontroller features to form the core of a very cost effective DRM radio receiver. Availability of software tools, support by experienced applications teams, and the required software modules and reference designs from third parties make this implementation a good choice for manufacturers in India and elsewhere to adopt the design and mass produce DRM radios that use it.

References

Feilen, Michael. "The Hitchhikers Guide to Digital Radio Mondiale (DRM)." *The Spark Modulator*, 2011.

Subrahmanyam, T.V.B., and Mohammed Chalil. "Emergence of High Performance Digital Radio." *Electronics Maker*, pp. 56-60, November 2012. www.electronicsmaker.com

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Modeling Amplifiers as Analog Filters Increases SPICE Simulation Speed

By David Karpaty

Introduction

Simulation models for amplifiers are typically implemented with resistors, capacitors, transistors, diodes, dependent and independent sources, and other analog components. An alternative approach uses a second-order approximation of the amplifier's behavior (Laplace transform), speeding up the simulation and reducing the simulation code to as little as three lines.

With high-bandwidth amplifiers, however, time-domain simulations using *s*-domain transfer functions can be very slow, as the simulator must first calculate the inverse transform and then convolve it with the input signal. The higher the bandwidth, the higher the sampling frequency required to determine the time-domain function. This results in increasingly difficult convolution calculations, slowing down the time-domain simulations.

This article presents a further refinement, synthesizing the second-order approximation as an analog filter rather than as an *s*-domain transfer function to provide much faster time-domain simulations, especially for higher bandwidth amplifiers.

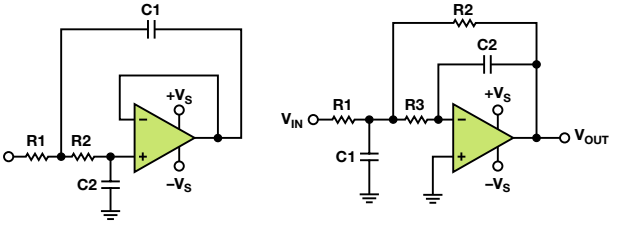
Second-Order Transfer Functions

The second-order transfer function can be implemented using the Sallen-Key filter topology, which requires two resistors, two capacitors, and a voltage-controlled current source for an amplifier simulation model; or the multiple feedback (MFB) filter topology, which requires three resistors, two capacitors, and a voltage-controlled current source. Both topologies should give the same results, but the Sallen-Key topology is simpler to design, while the MFB topology has better high-frequency response and might be better for programmable-gain amplifiers, as it is easier to switch in different resistor values.

We can begin the process by modeling the frequency and transient response of an amplifier with the following standard form for the second-order approximation:

$$\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Conversions to Sallen-Key and multiple feedback topologies are shown in Figure 1.



$$H_{LP} = \frac{\omega_c^2}{s^2 + \frac{\omega_c s}{Q} + \omega_c^2} \qquad H_{LP} = \frac{K\omega_c^2}{s^2 + \frac{\omega_c s}{Q} + \omega_c^2}$$

Figure 1 . Filter topologies.

The natural undamped frequency of the amplifier, ω_n, is equal to the corner frequency of the filter, ω_c, and the damping ratio of the amplifier, ζ, is equal to ½ times the reciprocal the quality factor of the filter, Q. For a two-pole filter, Q indicates the radial distance of the poles from the $j\omega$-axis, with higher values of Q indicating that the poles are closer to the $j\omega$-axis. With amplifiers, larger damping ratios result in lower peaking. These relationships serve as useful equivalencies between the *s*-domain ($s = j\omega$) transfer function and the analog filter circuit.

$$\omega_n = \omega_c$$

$$\zeta = \frac{1}{2Q}$$

Design Example: Gain-of-5 Amplifier

The design consists of three major steps: first, measure the amplifier's overshoot (M_p) and settling time (t_s). Second, using these measurements, calculate the second-order approximation of the amplifier's transfer function. Third, convert the transfer function to the analog filter topology to produce the amplifier's SPICE model.

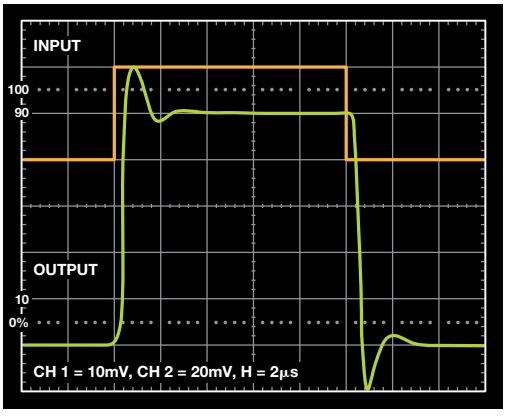


Figure 2. Gain-of-5 amplifier.

As an example, a gain-of-5 amplifier will be simulated using both Sallen-Key and MFB topologies. From Figure 2, the overshoot (M_p) is approximately 22%, and the settling time to 2% is approximately 2.18 µs. The damping ratio, ζ, is calculated as

$$M_p = e^{\frac{-\zeta\pi}{\sqrt{1-\zeta^2}}}$$

Rearranging terms to solve for ζ gives

$$\zeta = \sqrt{\frac{[\ln(M_p)]^2}{\pi^2 + [\ln(M_p)]^2}} = 0.434$$

Next, calculate the natural undamped frequency in radians per second using the settling time.

$$\omega_n = \frac{4}{t_s\zeta} = 4.226 \times 10^6$$

For a step input, the s^2 and s terms in the denominator of the transfer function (in radians per second) are calculated from

$$\omega_n^2 = \left(\frac{4}{t_s\zeta}\right)^2 = 17.861 \times 10^{12}$$

and

$$2\zeta\omega_n = 3.670 \times 10^6$$

The unity-gain transfer function then becomes

$$\frac{17.874 \times 10^{12}}{s^2 + 3.670 \times 10^6\, s + 17.874 \times 10^{12}}$$

The final transfer function for a gain-of-5 amplifier is obtained by multiplying the step function by 5:

$$5\times \frac{17.874 \times 10^{12}}{s^2 + 3.670 \times 10^6\, s + 17.874 \times 10^{12}}$$

$$= \frac{89.371 \times 10^{12}}{s^2 + 3.670 \times 10^6\, s + 17.874 \times 10^{12}}$$

The following netlist simulates the Laplace transform for the transfer function of the gain-of-5 amplifier. Before converting to a filter topology, it's good to run simulations to verify the Laplace transform, adjusting the bandwidth as needed by making the settling time larger or smaller.

```
***GAIN_OF_5 TRANSFER FUNCTION***
.SUBCKT SECOND_ORDER +IN -IN OUT
 E1 OUT 0 LAPLACE {V(+IN) - V(-IN)} =
{89.371E12 / (S^2 + 3.670E6*S + 17.874E12)}
.END
```

Figure 3 shows the simulation results in the time domain. Figure 4 shows the results in the frequency domain.

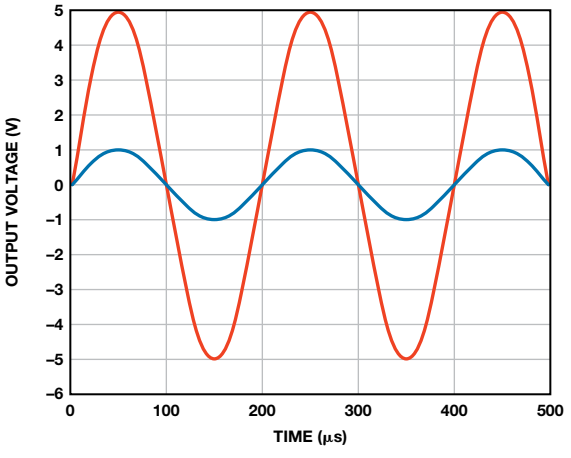


Figure 3. Gain-of-5 amplifier: time domain simulation results.

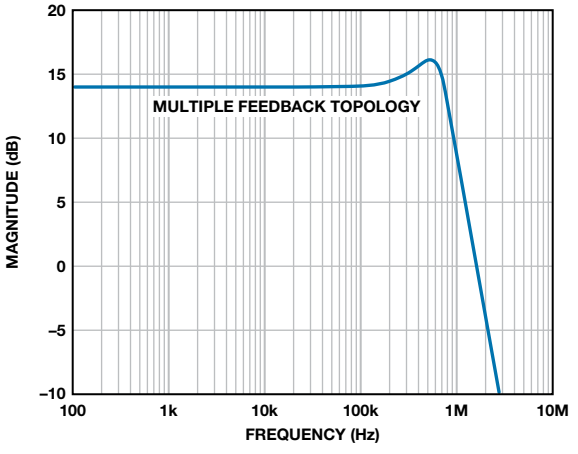


Figure 4. Gain-of-5 amplifier: frequency domain simulation results.

The peaking in the pulse response makes it easy to maintain a constant damping ratio while varying the settling time to modify the bandwidth. This changes the angle of the complex-conjugate pole pair with respect to the real axis in an amount equal to the arccosine of the damping ratio, as shown in Figure 5. Decreasing the settling time increases the bandwidth; and increasing the settling time decreases the bandwidth. Peaking and gain will not be affected as long as the damping ratio is kept constant and adjustments are made only to the settling time, as shown in Figure 6.

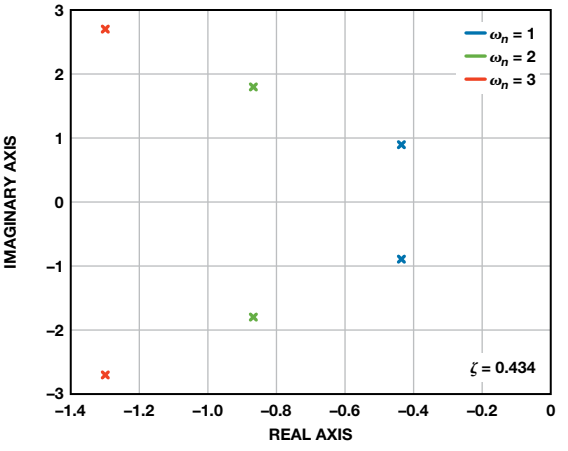


Figure 5. Complex conjugate pole-pair of the gain-of-5 transfer function.

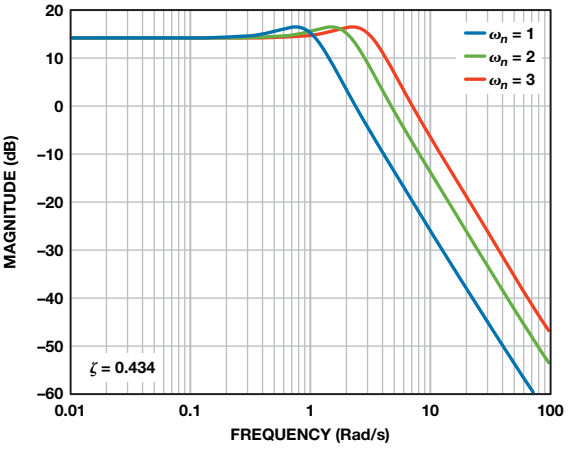


Figure 6. Bandwidth due to settling time adjustment.

Once the transfer function matches the characteristics of the actual amplifier, it is ready to be converted to a filter topology. This example will use both Sallen-Key and MFB topologies.

First, use the canonical form for the unity-gain Sallen-Key topology to convert the transfer function into resistor and capacitor values.

$$\frac{\frac{1}{R_1R_2C_1C_2}}{s^2 + \frac{(R_1 + R_2)}{R_1R_2C_1}\, s + \frac{1}{R_1R_2C_1C_2}}$$

From the s-term, C_1 can be found from

$$\frac{(R_1 + R_2)}{R_1R_2C_1}\, s = 3.670 \times 10^6$$

Choose convenient resistor values, such as 10 kΩ, for R_1 and R_2, and calculate C_1.

$$C_1 = \frac{(R_1 + R_2)}{2\zeta\omega_n R_1 R_2}\, s = 54.5 \times 10^{-12}$$

Use the relationship for the corner frequency to solve for C_2.

$$\omega_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$C_2 = \frac{1}{R_1 R_2 C_1 \omega_c{}^2} = 10.27 \times 10^{-12}$$

The resulting netlist follows, and the Sallen-Key circuit is illustrated in Figure 7. E1 multiplies the step function to obtain a gain of 5. *Ro* provides an output impedance of 2 Ω. G1 is a VCCS with a gain of 120 dB. E2 is the differential input block. The frequency vs. gain simulation was identical to the simulation using the Laplace transform.

```
.SUBCKT SALLEN_KEY +IN -IN OUT
R1 1 4 10E3
R2 5 1 10E3
C2 5 0 10.27E-12
C1 2 1 54.5E-12
G1 0 2 5 2 1E6
E2 4 0 +IN -IN 1
E1 3 0 2 0 5
RO OUT 3 2
.END
```

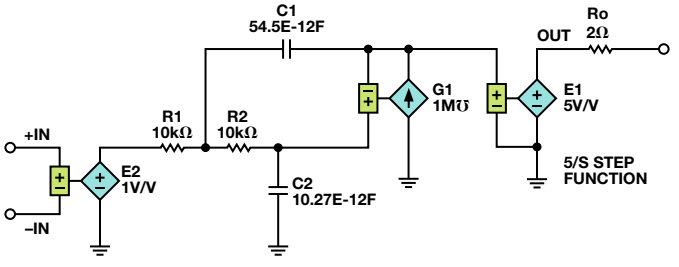


Figure 7. Simulation circuit for gain-of-5 amplifier using Sallen-Key filter.

Next, use the standard form for the MFB topology to convert the transfer function into resistor and capacitor values.

$$\frac{\dfrac{1}{R_1 R_3 C_1 C_2}}{s^2 + \left(\dfrac{(R_2 + R_3)}{R_2 R_3 C_1} + \dfrac{1}{R_1 C_1}\right) s + \dfrac{1}{R_2 R_3 C\, C_2}}$$

Begin the transformation by calculating R_2. To do this, the transfer function can be restated in this more generic form

$$\frac{Ka_0}{s^2 + a_1 s + a_0}$$

Set C_1 = 10 nF. Next, choose C_2 such that the quantity under the radical is positive. For convenience, C_2 was chosen as 10 pF.

Substituting the known values of C_2 = 10 pF, a_1 = 3.67E6, K = 5, and a_0 = 17.86E12 gives the value for R_2:

$$R_2 = \frac{2(1 + K)}{a_1 + \sqrt{a_1{}^2 - 4C2a_0(1 + K)}}$$

$$R_2 = \frac{2(1 + 5)}{3.67E6 + \sqrt{3.67E2 - (4 \times 1E - 11 \times 17.86E12 \times (1 + 5))}} = 165\Omega$$

R_1 can easily be found as $R_2/K = R_2/5 = 33$. From the standard polynomial coefficients, solve for R_3. Substituting known values for a_0, R_2, and C_2 gives

$$R_3 = \frac{1}{a_0 R_2 C_2} = 3.4\ \text{k}\Omega$$

Finally, to verify that the component ratios are correct, C_1 should equal 10 nF after substituting known values for a_0, R_2, R_3, gain K, and C_2 (from the s term).

$$C_1 = \frac{1}{a_0 R_2 R_3 C_2} = \frac{1}{a_0 R_1 R_3 C_2 K} = 10\ \text{nF}$$

Now that the component values are solved, substitute back into the equations to verify that the polynomial coefficients are mathematically correct. A spreadsheet calculator is an easy way to do this. The component values shown provide practical values for use in the final SPICE model. In practice, ensure that the minimum capacitor value does not fall below 10 pF.

The netlist for the gain-of-5 amplifier follows and the model is shown in Figure 8. G1 is a VCCS (voltage-controlled current source) with an open-loop gain of 120 dB. Note that the component count is much lower than would otherwise be required with transistors, capacitors, diodes, and dependent sources.

```
.SUBCKT MFB +IN -IN OUT
***VCCS - 120 dB OPEN_LOOP_GAIN***
G1 0 7 0 6 1E6
R1 4 3 330
R3 6 4 34K
C2 7 6 1P
C1 0 4 1N
R2 7 4 1.65K
E2 3 0 +IN -IN 1
E1 9 0 7 0 -1
***OUTPUT_IMPEDANCE RO = 2 Ω***
RO OUT 9 2
.END
```

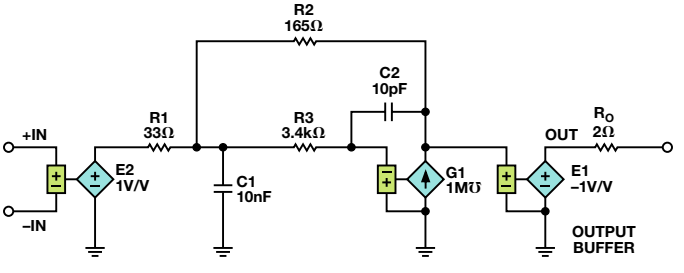


Figure 8. Simulation circuit for gain-of-5 amplifier using MFB filter.

Design Example: Gain-of-10 Amplifier

As a second example, consider the pulse response of a gain-of-10 amplifier without overshoot, as shown in Figure 9. The settling time is approximately 7 µs. Since there is no overshoot, the pulse response can be approximated as being critically damped, with $\zeta \approx 0.935$ ($M_p = 0.025\%$).

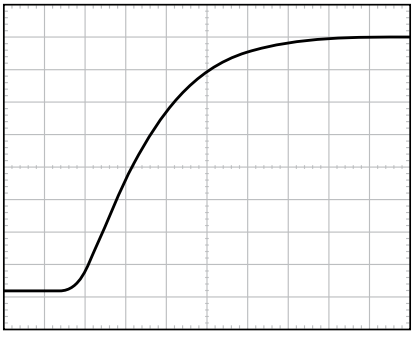


Figure 9. Gain-of-10 amplifier with no overshoot.

With no overshoot, it is convenient to maintain a constant settling time and adjust the damping ratio to simulate the correct bandwidth and peaking. Figure 10 shows how the poles move as the damping ratio is varied while maintaining a constant settling time. Figure 11 shows the change in frequency response.

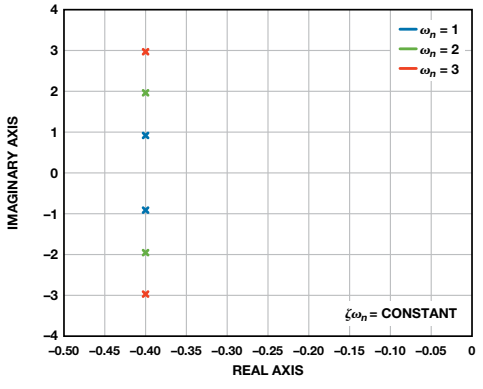


Figure 10. Pole locations for different damping ratios with constant setting time.

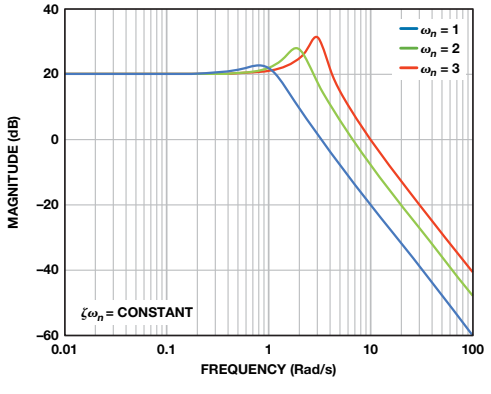


Figure 11. Frequency response for different damping ratios with constant setting time.

```
***AD8208 PREAMPLIFIER_TRANSFER_FUNCTION
(GAIN = 20 dB)***
.SUBCKT PREAMPLIFIER_GAIN_10 +IN -IN OUT
E1 OUT 0 LAPLACE {V(+IN)-V(-IN)} =
{3.734E12 / (S^2 + 1.143E6*S + 373.379E9)}
.END
```

To find resistor and capacitor values for the unity gain Sallen-Key topology, choose $R_1 = R_2 = 10$ kΩ as before. Calculate the capacitor values with the same method used in the gain-of-5 amplifier example:

$$\frac{(R_1 + R_2)}{R_1 R_2 C_1} s = 1.143 \times 10^6$$

$$C_1 = \frac{(R_1 + R_2)}{2\zeta\omega_n R_1 R_2} s = 175 \times 10^{-12},\ R_1 = R_2 = 10\ \text{k}\Omega$$

$$\omega_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$C_2 = \frac{1}{R_1 R_2 C_1 \omega_c^2} = 153 \times 10^{-12}$$

The netlist follows and the Sallen-Key simulation circuit model is shown in Figure 12. E2, a gain-of-10 block, is placed at the output stage along with a 2-Ω output impedance. E2 multiplies the unity gain transfer function by 10. Both Laplace and Sallen-Key netlists produced identical simulations, as shown in Figure 13.

```
***AD8208 PREAMPLIFIER_TRANSFER_FUNCTION
(GAIN = 20 dB)***
.SUBCKT AMPLIFIER_GAIN_10_SALLEN_KEY +IN
-IN OUT
 R1 1 4 10E3
 R2 5 1 10E3
 C2 5 0 153E-12
 C1 2 1 175E-12
 G1 0 2 5 2 1E6
 E2 4 0 +IN -IN 10
 E1 3 0 2 0 1
 RO OUT 3 2
.END
```

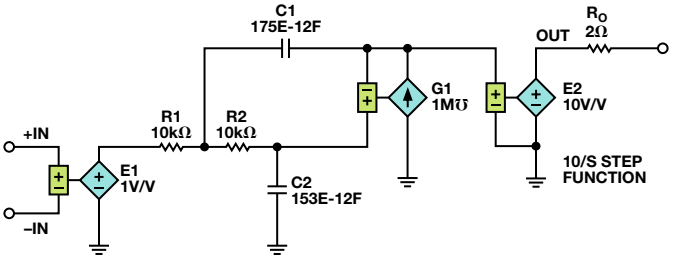


Figure 12. Simulation circuit for gain-of-10 amplifier using Sallen-Key filter.

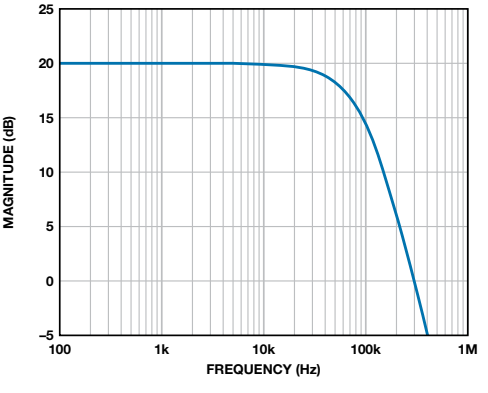


Figure 13. Frequency domain simulation of gain-of-10 amplifier using Sallen-Key filter.

A similar derivation can be done using the MFB topology. The netlist follows, and the simulation model is shown in Figure 14.

```
***AD8208 PREAMPLIFIER_TRANSFER_FUNCTION
(GAIN = 20 dB)***
.SUBCKT 8208_MFB +IN -IN OUT
***G1 = VCCS WITH 120 dB OPEN_LOOP_GAIN***
G1 0 7 0 6 1E6
R1 4 3 994.7
R2 7 4 9.95K
R3 6 4 26.93K
C1 0 4 1N
C2 7 6 10P
EIN_STAGE 3 0 +IN -IN 1
***E2 = OUTPUT BUFFER***
E2 9 0 7 0 1
***OUTPUT RESISTANCE = 2 Ω***
RO OUT 9 2
.END
```

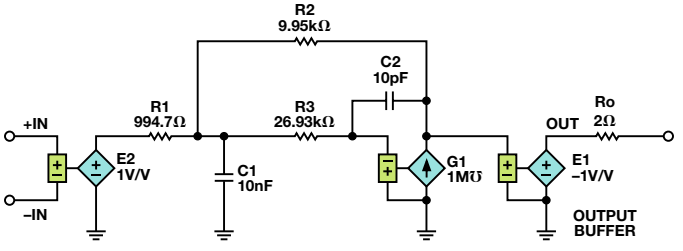


Figure 14. Simulation circuit for gain-of-10 amplifier using MFB filter.

Conclusion

SPICE models constructed with analog components will provide much faster time-domain simulations for higher bandwidth amplifiers as compared to those of *s*-domain (Laplace transform) transfer functions. The Sallen-Key and MFB low-pass filter topologies provide a method for converting *s*-domain transfer functions into resistors, capacitors, and voltage-controlled-current-sources.

Non-ideal operation of the MFB topology results from C_1 and C_2 behaving as shorts at high frequencies relative to the impedance of resistors R_1, R_2, and R_3. Similarly, non-ideal operation of the Sallen-Key topology results from C_1 and C_2 behaving as shorts at high frequencies relative to the impedance of resistors R_1 and R_2. A comparison of the two topologies is shown in Figure 15.

Existing circuits commonly used for CMRR, PSRR, offset voltage, supply current, spectral noise, input/output limiting, and other parameters can be combined with the model, as shown in Figure 16.

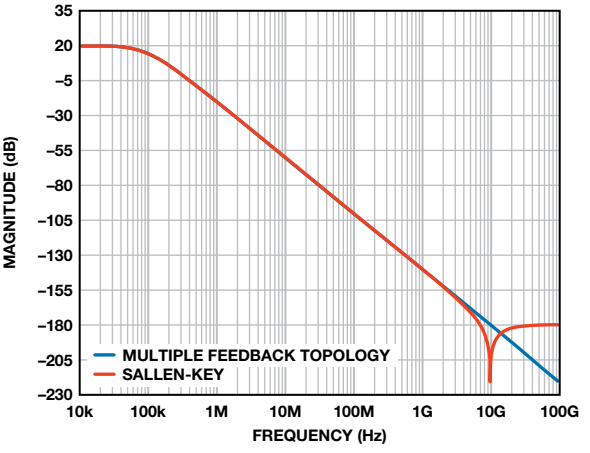


Figure 15. Bode plots of Sallen-Key and MFB topologies.

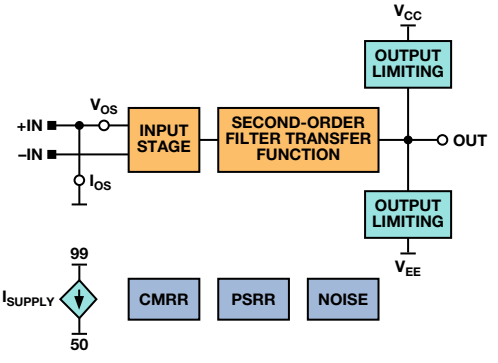


Figure 16. Complete SPICE amplifier model including error terms.

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Karpaty, David. "Create Spice Amplifier Models Using Second-Order Approximations." *Electronic Design*, September 22, 2010.

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Convert a Buck Regulator into a Smart LED Driver, Including Dimming

By Jon Kraft

With their long lives and low energy consumption, LEDs promise to change the lighting industry, but a key limiter to rapid adoption is the cost of the LEDs themselves. The cost of LED *luminaires* (complete electric light units) varies, but the cost of the LED, typically around 25% to 40% of the total luminaire cost, is projected to remain significant for many years (Figure 1).

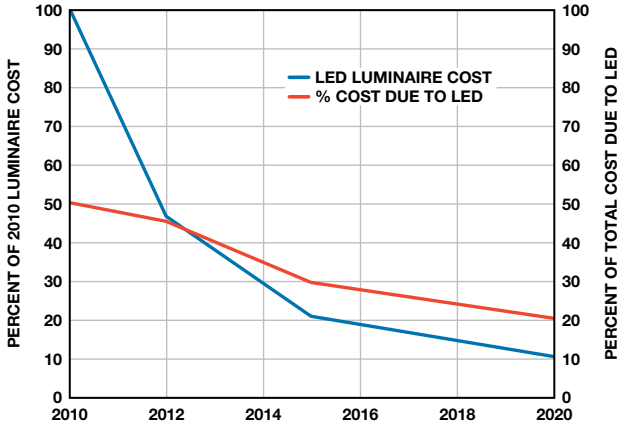

Figure 1. Breakdown of LED luminaire costs.[1]

One way to reduce the total luminaire cost is to drive the LED at up to its highest possible dc current, as allowed in its datasheet. This may be considerably higher than its "binning current." If driven properly, this can produce greater lumens/cost.

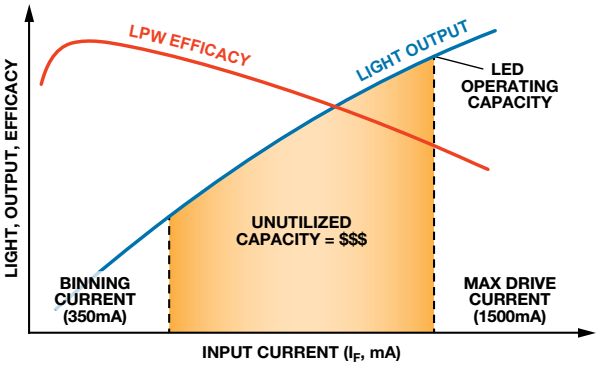

Figure 2. LED light output and efficacy vs. drive current.[2]

However, doing this requires higher current drivers. Many solutions are available for driving LEDs at low currents (<500 mA), but fewer options exist at higher currents (700 mA to 4 A). This may seem surprising, given that the semiconductor world is rich with dc-to-dc solutions having capacities up to 4 A, but these are designed to control *voltage*, not LED *current*. This article examines some easy tricks to transform a readily available dc-to-dc buck regulator into a smart LED driver.

A buck regulator chops an input voltage and passes it through an LC filter to provide a stable output, as illustrated in Figure 3. It employs two active elements and two passive elements. The active elements are switch "A" from the input to the inductor, and switch (or diode) "B" from ground to the inductor. The passive elements are the inductor (L) and the output capacitor (C_{OUT}). These form an LC filter, which reduces the ripple created by the active elements.

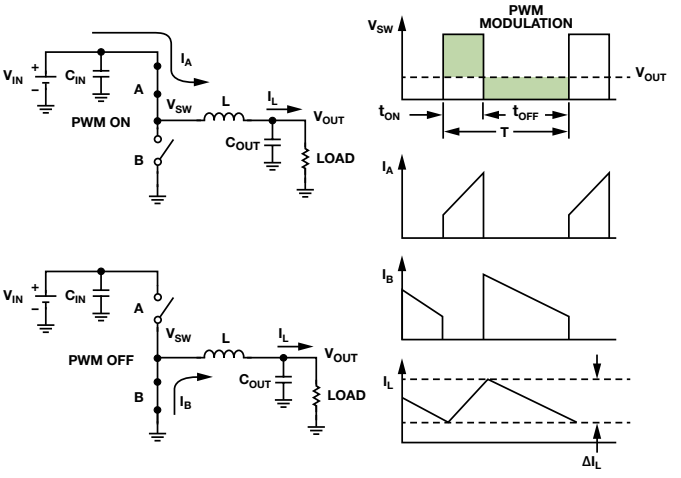

Figure 3. Basic buck arrangement.[3]

The buck is called a *regulator* if the switches are internal, or a *controller* if the switches are external. It's *synchronous* if both switches are transistors (MOSFETs or BJTs) or *asynchronous* if the bottom switch is implemented with a diode. Each of these categories of buck circuits has its own merits and drawbacks, but synchronous buck regulators typically optimize efficiency, parts count, solution cost, and board area. Unfortunately, synchronous buck regulators for driving high-current LEDs (up to 4 A) are few and expensive. Using the ADP2384 as an example, this article shows how to modify the connections of a standard synchronous buck regulator to regulate LED current.

The ADP2384 high-efficiency synchronous buck regulator specifies output current up to 4 A with an input voltage up to 20 V. Figure 4 shows its normal connections for regulating output voltage.

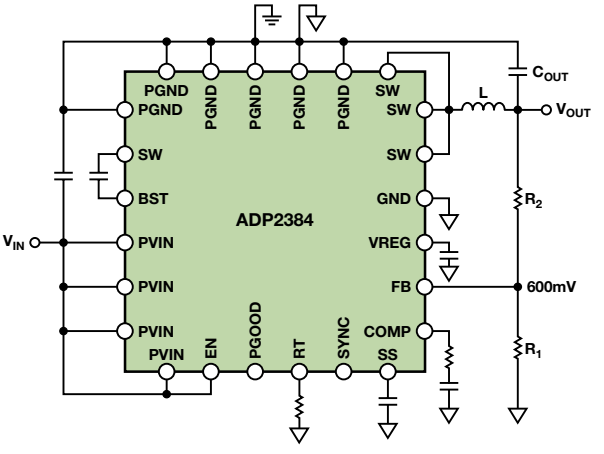

Figure 4. ADP2384 connected for regulating output voltage.

In operation, a divided down copy of the output voltage is connected to the FB pin, compared with an internal 600-mV reference, and used to generate the proper duty cycle to the switches. In the steady state, the FB pin is held at exactly 600 mV, so V_{OUT} is regulated at 600 mV times the division ratio. If the upper resistor is replaced by LEDs (Figure 5), the output voltage must be whatever is needed (within ratings) to maintain 600 mV at FB; therefore, the current through the LEDs will be controlled at 600 mV/R_{SENSE}.

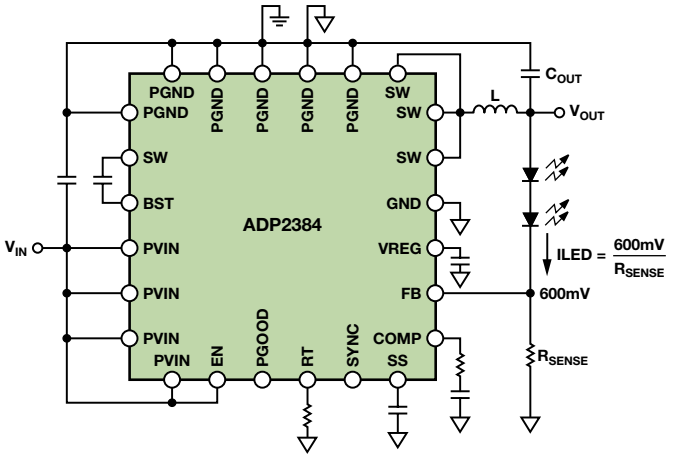

Figure 5. Basic (but inefficient) LED driver.

This circuit works nicely when a precision resistor from FB to ground sets the LED current, but the resistor dissipates a lot of power: P = 600 mV × I_{LED}. This is not a big issue for low LED currents, but at high LED currents, the low efficiency adds significantly to the heat dissipated by the luminaire (600 mV × 4 A = 2.4 W). Lowering the FB reference voltage reduces the power dissipation proportionally, but most dc-to-dc regulators do not have a means to adjust this reference. Fortunately, two tricks can reduce the reference voltage for most buck regulators: use the SS/TRK pin—or offset the R_{SENSE} voltage.

Many general-purpose buck ICs include a soft start (SS) or tracking (TRK) pin. The SS pin minimizes start-up transients by slowly increasing the switching duty cycle at startup. The TRK pin allows the buck regulator to follow an independent voltage. These functions are often combined onto a single SS/TRK pin. In most cases, the error amplifier will compare the smallest of the SS, TRK, and FB voltages with the reference, as shown in Figure 6.

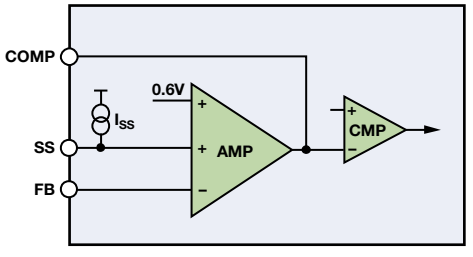

Figure 6. Soft start pin operation using the ADP2384.

For the luminaire application, set the SS/TRK pin to a fixed voltage and use it as the new FB reference. A divider from a constant voltage works nicely as a reference source. For example, many buck regulator ICs include a controlled low-voltage output—such as the V_{REG} pin on the ADP2384. For greater accuracy, a simple 2-terminal external precision reference, such as the ADR5040, can be used. In any case, a resistive divider from that supply to the SS/TRK pin forms the new reference. Setting this voltage to between 100 mV and 200 mV generally offers the best compromise between power dissipation and LED current accuracy. Another benefit of a user-chosen reference voltage is that R_{SENSE} can be chosen as a convenient standard value, avoiding the expense and inaccuracy of specifying or assembling an arbitrary precision resistance value to set the LED current.

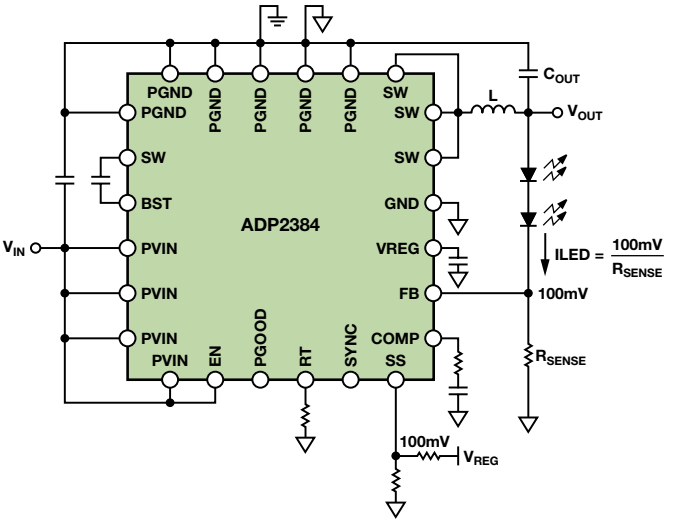

Figure 7. Using the SS/TRK pin to reduce the FB reference voltage.

Using the SS or TRK pin approach is not viable for all buck regulators, as some ICs do not have these pins. Also, with some buck ICs, the SS pin changes the peak inductor current, not the FB reference, so it is necessary to check the data sheet carefully. As an alternative, the R_{SENSE} voltage can be offset. For example, a resistive divider between an accurate voltage source and R_{SENSE} provides a fairly constant offset voltage from R_{SENSE} to the FB pin (Figure 8).

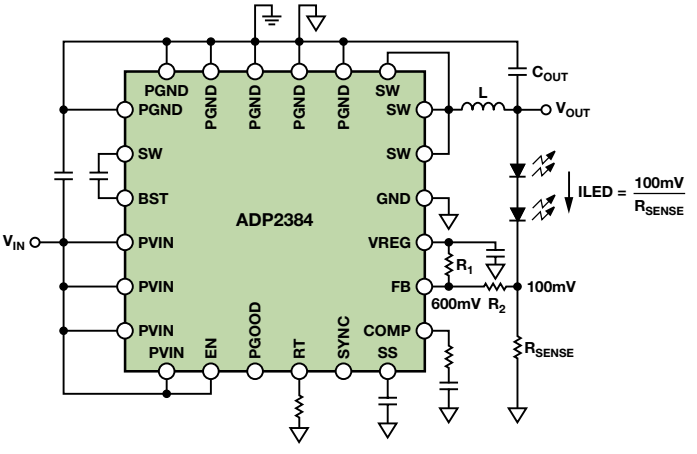

Figure 8. Offset the R_{SENSE} voltage.

The necessary values for the resistive divider can be found using Equation 1, where V_{SUP} is the auxiliary regulated voltage, and $FB_{REF(NEW)}$ is the desired voltage across R_{SENSE}.

$$R1 = R2 \times \frac{V_{SUP} - FB_{REF}}{FB_{REF} - FB_{REF(NEW)}}$$

So, to get an effective feedback reference of 150 mV, with $R2$ = 1 kΩ and V_{SUP} = 5 V:

$$R1 = 1\ k\Omega \times \frac{5.0\ V - 0.6\ V}{0.6\ V - 0.15\ V} = 9.78\ k\Omega$$

The LED current is:

$$I_{LED} = \frac{FB_{REF(NEW)}}{R_{SENSE}}$$

This approach does not require an SS or TRK pin. The FB pin will still regulate to 600 mV (but the voltage at R_{SENSE} regulates to $FB_{REF(NEW)}$). This means that other functions of the chip (including soft start, tracking, and power good) will still function normally.

A disadvantage of this method is that the offset between R_{SENSE} and FB is strongly influenced by the accuracy of the supply. Using a precision reference such as the ADR5040 would be ideal, but a less accurate reference tolerance of ±5% would create a ±12% variation in the LED current. A comparison is shown in Table 1:

Table 1. Comparison of SS/TRK and Offsetting R_{SENSE}

Option 1: Use SS/TRK to Reduce FB Reference	Option 2: Offset R_{SENSE} Voltage
±5% supply voltage variation gives ±5% error on I_{LED}. This is not impacted by the V_{SENSE} voltage; therefore, this method has the lowest R_{SENSE} power dissipation.	±5% supply voltage variation gives ±12% error on I_{LED}. Higher V_{SENSE} voltages improve this.
Very good open/short LED protection. FB_OVP does not factor into intermittent open protection. LED current is limited by the inductor and the control loop speed.	Very good open/short LED protection. Additionally, some ICs have another FB reference (FB_OVP) that immediately disables switching if FB rises 50 mV to 100 mV above normal. This guarantees the maximum LED overcurrent during intermittent faults.
PGOOD will always remain low.	Since FB pin still regulates to 600 mV, the PGOOD pin functions normally.
By keeping the SS/TRK pin lower than normal, some fault modes may not work properly.	All fault modes work normally.

Another key for accurate current regulation is proper layout routing to the sense resistor. A 4-terminal sense resistor is ideal, but can be expensive. Good layout techniques allow high accuracy to be obtained using a traditional 2-terminal resistor, as shown in Figure 9.[4]

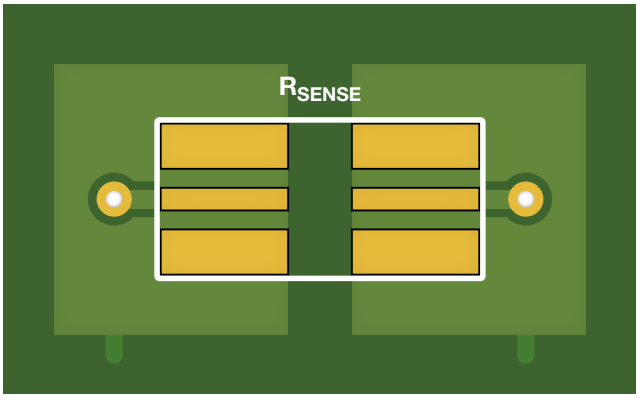

Figure 9. Recommended PCB trace-routing for R_{SENSE}.

Beyond Regulating

Regulating the LED current using an off-the-shelf buck regulator is straightforward. The examples shown here employ the ADP2384. A more-extensive paper also includes examples using the ADP2441, a device with fewer pins and a 36-V input voltage range. It shows examples illustrating how to implement many of the "smart" features that are available with dedicated LED buck regulators, such as LED short/open fault protection, R_{SENSE} open/short fault protection, PWM dimming, analog dimming, and current foldback thermal protection. We will discuss PWM and analog dimming, and current foldback here, using the ADP2384 as in the above examples.

Dimming with PWM and Analog Control

A key requirement for a "smart" LED driver is adjusting the LED brightness with *dimming* controls, using one of two approaches: PWM and analog. PWM dimming controls the LED current by adjusting the pulse duty cycle. If the frequency is above about 120 Hz, the human eye averages these pulses to produce a perceived average luminosity. Analog dimming scales the LED current at a constant (dc) value.

PWM dimming could be implemented by opening and closing an NMOS switch inserted in series with R_{SENSE}. These current levels would require a power device, but adding one of these would defeat the size and cost benefits obtained by using a buck regulator containing its own power switches. Alternatively, PWM dimming can be performed by quickly turning the regulator on and off. At low PWM frequencies (<1 kHz), this can still give great accuracy (Figure 10).

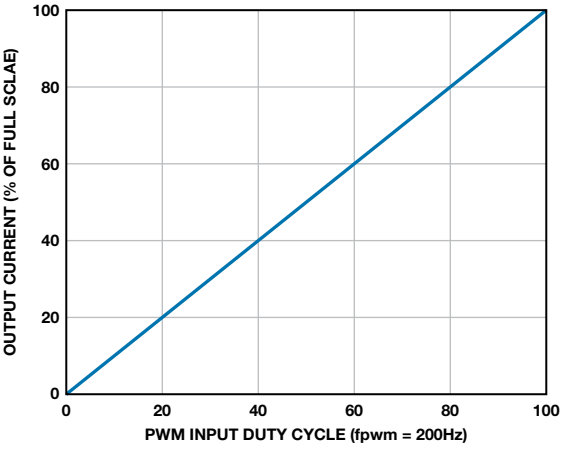

Figure 10. ADP2384 PWM dimming linearity—output current vs. duty cycle at 200 Hz.

Like all general-purpose buck regulators, the ADP2384 doesn't have a pin to apply a PWM dimming input, but the FB pin can be manipulated to enable and disable switching. If FB goes high, the error amplifier goes low, and the buck switching stops. If FB is reconnected to R_{SENSE}, then it resumes normal regulation. This can be done with either a low-current NMOS transistor or a general-purpose diode. In Figure 11, a high PWM signal connects R_{SENSE} to FB, enabling LED regulation. A low PWM signal turns the NMOS off, with a pull-up resistor bringing FB high.

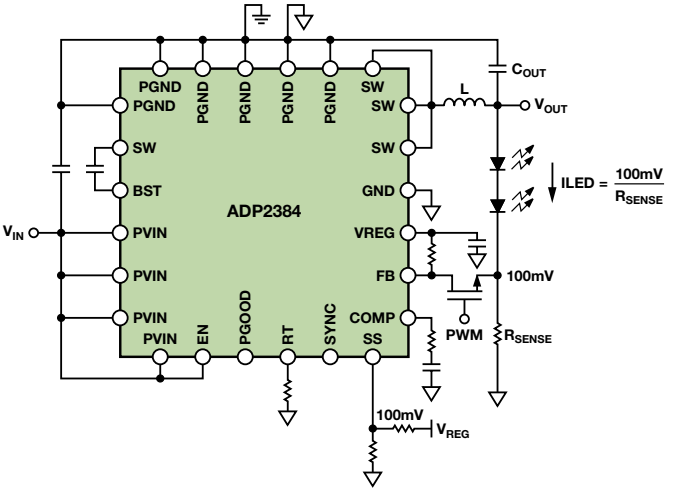

Figure 11. PWM dimming with the ADP2384.

PWM dimming is very popular, but sometimes noiseless "analog" dimming is required. Analog dimming simply scales the constant LED current, whereas PWM dimming chops it. Analog dimming is required if two dimming inputs are used, since multiple PWM dimming signals can create beat frequencies that cause flicker or audible noise. However, PWM might be used for one dimming control and analog for another. With a general-purpose buck regulator, the easiest way to implement analog dimming is to manipulate the FB reference by adjusting the supply for the FB reference circuit, as described in Figure 12.

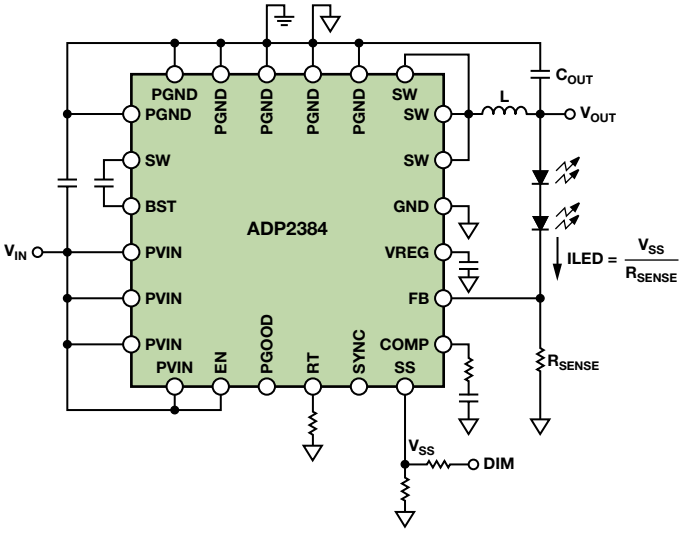

Figure 12. Analog dimming circuit.

Thermal Foldback

Since the lifetime of an LED is heavily dependent on its operating junction temperature, it is sometimes necessary to monitor the LED temperature and respond if the temperature is too high. An abnormally high temperature could be caused by a poorly connected heat sink, an unusually hot ambient, or some other extreme condition. A common solution is to reduce the LED current if the temperature exceeds some threshold (Figure 13). This is called LED *thermal foldback*.

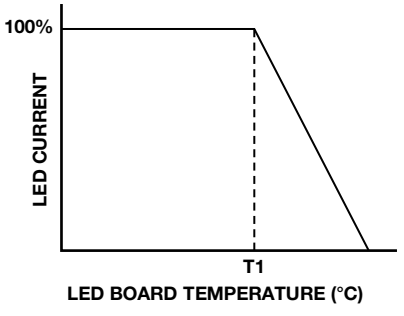

Figure 13. Desired LED thermal foldback curve.

In this type of dimming, the LEDs are kept at full current until a temperature threshold (T1) is reached, above which the LED current starts to decrease with increasing temperature. This limits the junction temperature of the LEDs and preserves their lifetime. A low cost NTC (negative temperature coefficient) resistor is commonly used to measure the LED's heat sink temperature.

With a small modification to the analog dimming scheme, the NTC's temperature can easily control the LED current. If the SS/TRK pin is used to control the FB reference, a simple method is to place the NTC in parallel with the reference voltage (Figure 14).

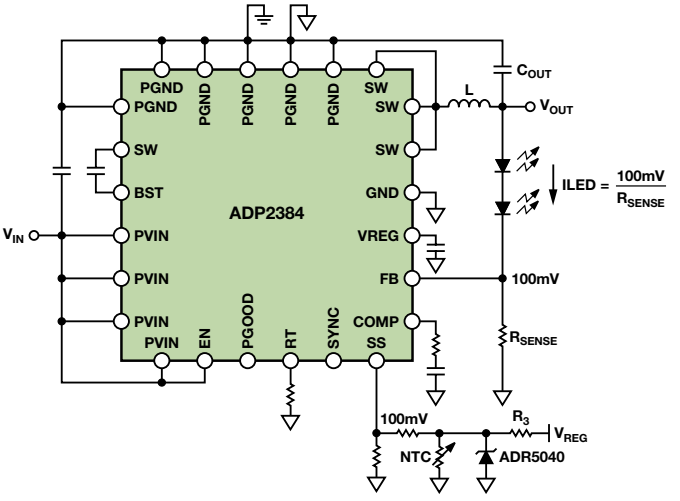

Figure 14. LED thermal foldback using the SS/TRK pin.

As the heat sink temperature rises, the NTC resistance drops. The NTC forms a resistive divider with R3. If the divider's voltage is above the reference voltage, maximum current is delivered; if the NTC resistor voltage drops below the reference voltage, then the FB reference voltage, and hence, the LED current, starts to drop.

Conclusion

These tips should be taken as general guidelines for implementing comprehensive LED features using a standard buck regulator. However, since these features are a little outside of the intended application for the buck IC, it is always best to contact the semiconductor manufacturer for assurance that the IC can handle these modes of operation. For more information on the ADP2384 and other buck regulators, such as the ADP2441, or for demo boards of these LED driver solutions, please visit www.analog.com/lighting.

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[1]DOE SSL 2011 Manufacturing Roadmap. http://ssl.energy.gov.

[2]Cox, David, Don Hirsh, and Michael McClintic. "Are you using all of the lumens that you paid for?" *LED Magazine*, Feb. 2012.

[3]Marasco, Ken. "How to Apply DC-to-DC Step-Down (Buck) Regulators Successfully." *Analog Dialogue*, Vol. 45, No. 2 (2011).

[4]O'Sullivan, Marcus. "Optimize High-Current Sensing Accuracy by Improving Pad Layout of Low-Value Shunt Resistors." *Analog Dialogue*, Vol. 46, No. 2 (2012).

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Understanding How Amplifier Noise Contributes to Total Noise in ADC Signal Chains

By Umesh Jayamohan

Introduction

Analog-to-digital converters (ADCs) provide optimal performance when the analog inputs are driven to their rated full-scale input voltage, but in many applications, the maximum available signal differs from the specified voltage and may need to be adjusted. A useful device for handling this requirement is a *variable-gain amplifier* (VGA). Understanding how the VGA affects the ADC's performance will help in optimizing performance of the entire signal chain.

This article analyzes noise in a circuit that uses the AD9268 dual 16-bit, 125-/105-/80-MSPS, pipelined ADC, and the AD8375 ultralow distortion IF VGA. The signal chain includes a VGA—used at a gain setting of +6 dB, a 5th-order Butterworth low-pass filter with a –3-dB roll-off at 100 MHz, and the ADC. Noise calculations will be shown for the amplifier and filter, as they dictate the dynamic performance of the ADC over the band of interest.

Problem

Many real-world applications using high-speed ADCs need some sort of driver, amplifier, or gain block that scales the input signal to the full-scale analog input range[1] to ensure optimum *signal-to-noise ratio* (SNR) and spurious-free dynamic range (SFDR). In addition, a differential amplifier could also convert a single-ended signal to a differential signal to drive the ADC. Being *active*, these components contribute noise at the ADC front end. The integration of this noise over the operational bandwidth will degrade the conversion performance.

The choice of an appropriate ADC for an application depends on *many factors*, including:

- Analog input range
- Input frequency/bandwidth
- Desired resolution/SNR
- Desired SFDR

Some applications require both high dynamic range and high resolution. The AD9268 is very good choice for these applications, delivering 78.2-dBFS (dB relative to full-scale) SNR and 88-dBc SFDR at a 70-MHz intermediate frequency.

At the system level, the ADC front-end could use an amplifier, a transformer, or a balun, but implementations using an amplifier are most common. An amplifier could be used for one or more of the following reasons:

- Provide gain to the input signal to increase the ADC resolution.
- Buffer or transform the impedance between the input source and the ADC.
- Convert a single-ended input signal to a differential output signal.

The AD8375 VGA, which maintains high linearity and uniform noise performance over its various gain settings, can be used to convert single-ended signals to differential. These characteristics make it a good candidate for driving the ADC at higher intermediate frequencies. Unfortunately, the presence of an active device—the amplifier—in the signal chain can limit the ADC's performance.

Example

Figure 1 shows the circuit topology used in performing the noise calculations. The AD8375 has a high-impedance differential output (16 kΩ||0.8 pF). A 5th-order low-pass antialiasing filter (AAF) with 100-MHz bandwidth and 150-Ω input and output impedances interfaces the amplifier to the ADC. The frequency response of the circuit shown in Figure 1 can be seen in Figure 2.

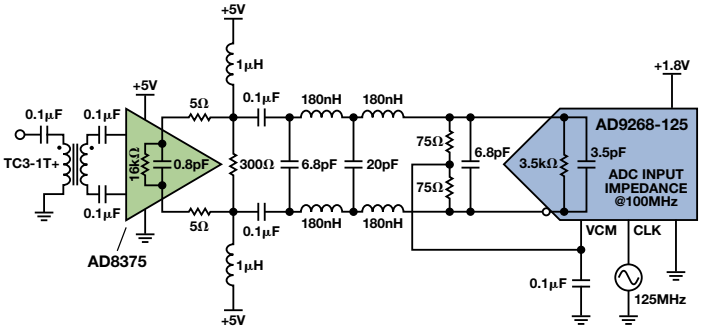

Figure 1. The AD8375, AAF, and AD9268 signal chain.

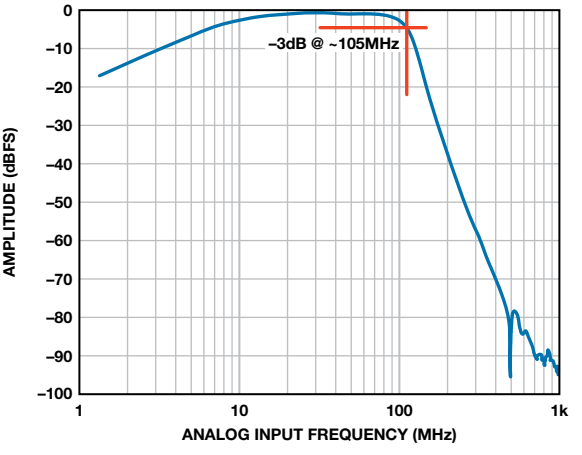

Figure 2. Frequency response of the AD8375, AAF, and AD9268 signal chain.

Performance

System designers may not expect the amplifier driving the ADC inputs to degrade the overall dynamic performance of the system, but the fact that a driver and ADC combo was chosen for one application does not mean that it will provide the same great performance in another application. The technique described here allows a systems engineer to estimate the expected performance before choosing an amplifier.

Figure 3 shows two different setups: Figure 3(a), which uses passive coupling to the converter, is available as the default option on the customer evaluation board. The *passive* front-end network uses a transformer or balun to convert the single-ended signal to differential, along with a passive low-pass filter that rolls off at about 200 MHz. Figure 3(b) shows the optional *amplifier* path. A comparison of the noise contributed by these two setups follows. A single-tone *fast Fourier transform* (FFT) at a low intermediate frequency (10 MHz) is used to calculate the noise added by the amplifier.

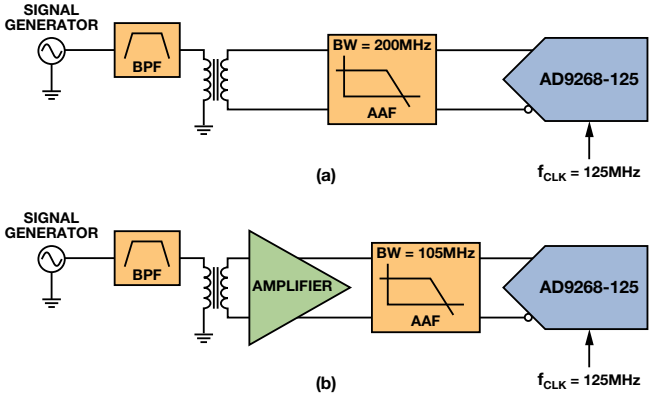

Figure 3. Typical ADC front-ends: (a) passive. (b) active.

Two techniques are typically used for analyzing the noise, but each can be cumbersome. *Noise spectral density* (NSD) defines the noise power per unit bandwidth. It is represented in mean-square dBm/Hz or dBFS/Hz for ADCs and rms nV/$\sqrt{\text{Hz}}$ for amplifiers. This incompatibility in units provides an obstacle to calculating system noise when an amplifier is driving an ADC.

Noise figure (NF) is the log ratio of input SNR to the output SNR expressed in decibels. This specification, commonly used by RF engineers, makes sense in a purely RF world, but attempting to use NF calculations in a signal chain with an ADC can lead to misleading results.[2]

An alternate, but more effective, technique is to "de-normalize" the noise density, representing it as an rms noise voltage rather than a mean-square voltage. This method, as described here, is straightforward and allows a clear analysis of the system noise.

Figure 4 and Figure 5 show the low-frequency single-tone FFTs of the two front ends. Note that the passive front end has 77.7-dBFS SNR, while the active front end has 72.5-dBFS SNR, 5.2 dBFS lower than the ADC's expected performance.

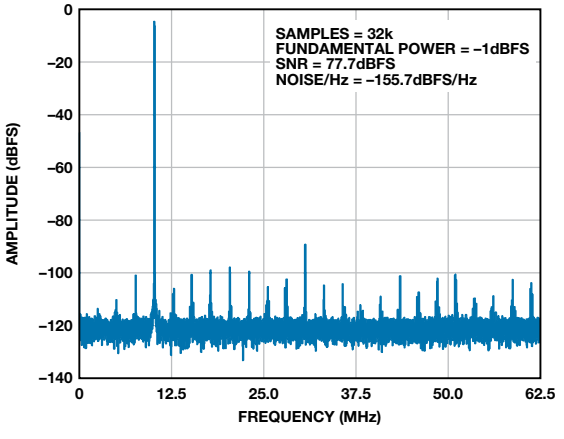

Figure 4. FFT of a 10-MHz analog input tone for the circuit of Figure 3a.

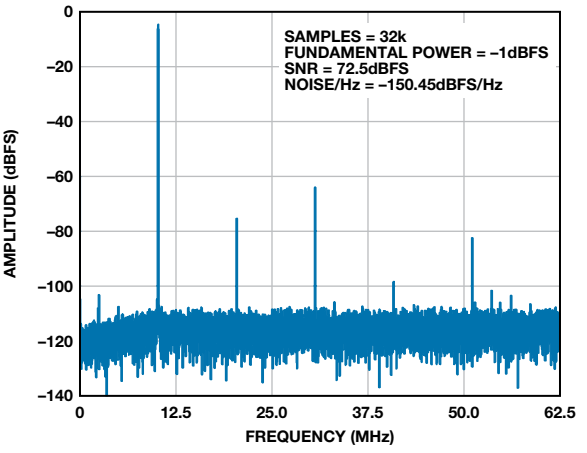

Figure 5. FFT of a 10-MHz analog input tone for the circuit of Figure 3b.

Analysis

The only difference between the setups shown in Figure 3a and 3b is the addition of the amplifier in the signal chain, so it is safe to assume that the performance degradation is caused by the amplifier's noise. The following calculations help to understand the additional noise introduced by the amplifier.

First, use the converter's full-scale differential input voltage, as specified in the data sheet. Convert the peak-to-peak voltage to rms by dividing by $2\sqrt{2}$ to get 0.707 V rms.

$$V_{RMS} = \frac{V_{pp}}{2\sqrt{2}} \tag{1}$$

The contribution of the converter's noise based on the ADC's typical SNR at 10 MHz is

$$SNR = 20 \log \left(\frac{V_{FS,\,RMS}}{V_{NOISE,\,RMS}} \right) dBFS \tag{2}$$

$$V_{NOISE,\,RMS} = \frac{V_{FS,\,RMS}}{10^{\left(\frac{SNR}{20}\right)}} \tag{3}$$

$$V_{NOISE,\,ADC} = 92.2\,\mu V_{RMS}$$

Using $V_{NOISE,\,ADC}$ = 92.2 µV rms and system SNR with the amplifier front end = 72.5 dBFS, the system noise, using Equation 3, is 168 µV rms.

$$V_{NOISE,\,TOTAL} = \frac{0.707}{10^{\left(\frac{72.5}{20}\right)}} = 168\,\mu V_{RMS} \tag{4}$$

$$V_{NOISE,\,TOTAL} = \sqrt{\left(V_{NOISE,\,AMP}\right)^2 + \left(V_{NOISE,\,ADC}\right)^2} \tag{5}$$

$$V_{NOISE,\,AMP} = 140\,\mu V_{RMS}$$

The system noise obtained from Equation 4 is the combined noise of the ADC and the VGA. The amplifier noise can be calculated from Equation 5 to be 140 μV rms. This calculation shows that the amplifier noise is at least 50% greater than the ADC noise, making it the limiting factor in determining the system's ac performance.

Note that we must determine whether the value of $V_{NOISE,\ AMP}$ calculated above matches the amplifier's data sheet. The specified noise spectral density is about 20 nV/√Hz with a 150-Ω differential output impedance.

Although the data sheet specifies that the VGA's noise is fairly constant with gain, this noise will change with the load, so the noise spectral density should be scaled to the total impedance driven by the amplifier outputs. Because the differential output impedance of the amplifier is large (16 kΩ||0.8 pF), the impedance seen by the amplifier (see Figure 1) can be calculated as

$$[10\ \Omega + (300\ \Omega||150\ \Omega||3.5\ k\Omega)] = 107\ \Omega.$$

Using this number, the derated noise spectral density for the AD8375 in this application can be found from Equation 6:

$$AmplifierNSD = 20\frac{nV}{\sqrt{Hz}} \times \frac{107}{150} = 14.3\frac{nV}{\sqrt{Hz}}$$

$$V_{NOISE,\ AMP}(Calculated) = NSD\left(\frac{nV}{\sqrt{Hz}}\right) \times \sqrt{BW \times ShapeFactor} \quad (6)$$

Note that when calculating system noise using a real filter, the noise bandwidth takes on a different shape than that of an ideal filter. This deviation in frequency response is characterized by the term, *shape factor,* and accounts for the noise in the roll-off region. The shape factor, which depends on the order of the filter, is the ratio of the noise bandwidth to the –3-dB bandwidth.[3] The more poles in the filter, the closer the shape factor is to unity. This relationship can be seen in Table 1.

Table 1. Relationship Between System Order and Shape Factor

System Order	Shape Factor
1	1.57
2	1.11
3	1.05
4	1.03
5	1.02

In the example of Figure 1, the shape factor is 1.02. Using Equation 6, the noise injected by the amplifier will be;

$$V_{NOISE,\ AMP}(Calculated) = 14.3\frac{nV}{\sqrt{Hz}} \times \sqrt{105\ MHz} \times 1.02 = 149\ \mu V_{RMS}$$

$$V_{NOISE,\ AMP}(Calculated) = 149\ \mu V_{RMS}$$

This estimated value of noise injected into the system by the VGA matches very well with the measured value using Equation 5, proving that the performance of the signal chain comprising the AD8375 and AD9268 is dominated by the amplifier.

Conclusion

In many cases, an amplifier—VGA or gain block—is required to drive a full-scale signal to an ADC in the system signal chain. The systems designer must be aware of the degradation in optimal performance of the ADC caused by the choice of the amplifier. Before designing with the chosen amplifier and ADC, the designer can use the method shown here to calculate the noise contribution of the amplifier to estimate the expected dynamic performance, as characterized by the SNR, for the intended system implementation.

References

[1] MT-006, *ADC Noise Figure—An Often Misunderstood and Misinterpreted Specification.*

[2] *The Data Conversion Handbook.*

[3] Reeder, Rob and Jim Caserta, "Ask The Application Engineer 36, Wideband A/D Converter Front-End Design Considerations II: Amplifier-or Transformer Drive for the ADC?" *Analog Dialogue* 41-02, 2007.

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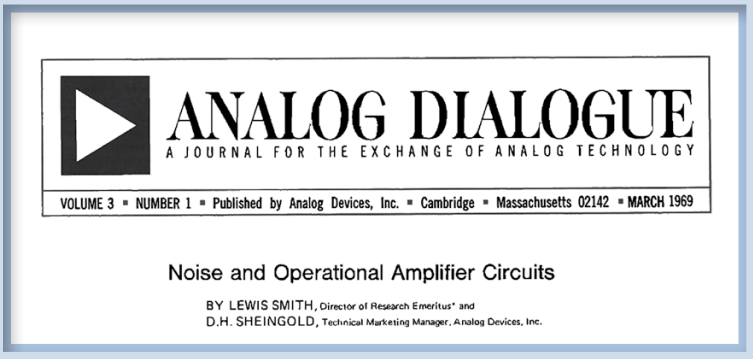
ANALOG DIALOGUE
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Noise and Operational Amplifier Circuits
BY LEWIS SMITH, Director of Research Emeritus* and
D.H. SHEINGOLD, Technical Marketing Manager, Analog Devices, Inc.

We have one person who is being recognized for 40 years of service. Dan Sheingold joined ADI in 1969.

This was a very fertile period in ADI's history as we went public, acquired Pastoriza as a platform to enter the converter market, and launched Nova Devices to begin our journey into ICs. But it is also noteworthy that I persuaded Dan to join ADI as the editor of *Analog Dialogue*. When I learned that Philbrick, the pioneer of op amps as functional building blocks, had been acquired, I went after Dan where he had been successful in launching *Analog Monologue* and creating the image of Philbrick as the innovation leader in this emerging market. After 19 years at Philbrick, Dan joined ADI, and for the next 40 years established *Analog Dialogue* as the longest surviving industry published technical journal.

Analog Dialogue, through Dan's insight into technical and market trends, and through his mastery of the English language, played a pivotal role in our success by building ADI's image as the technical leader in analog products and technology and by helping our customers understand and apply the tremendous outpouring of technical innovations from the company over four decades. Thanks Dan for joining me at Jimmy's Harborside restaurant in December 1968 and accepting our offer to join ADI.

Ray Stata, Chairman of the Board, Analog Devices
June 2009

A Tribute to Dan Sheingold

I wouldn't say that Dan is old, but when he first came to Analog, the only things that were monolithic were the tablets he chiseled to make *Analog Dialogue.*

And I wouldn't say that Dan is behind the times, but he still thinks that Twitter is what nervous teens do at the prom.

And, I wouldn't say that Dan served in the same role too long, but after working on *Dialogue* for 14 years, I was starting to feel like Prince Charles waiting for Queen Elizabeth to abdicate the throne.

What I would say, though, is that Dan taught me a love of words—how technical topics could be presented in a clear yet compelling fashion, and with a minimum of hype. Dan also taught me that someone could love his career so much that he still looked forward to coming to work—and was still an invaluable asset—even after 44 years. And, in addition to being eager to teach, Dan was also eager to learn, listening to and trying new ideas in his constant quest to improve himself, his department, and our magazine. This, too, was an important lesson.

As Dan moves into the next phase of his life, I know that he's not going to rest. If he still has time after singing in his chorus, reading to the blind, and visiting with his family, I hear that Energizer® might have an opening to replace their tired old bunny.

Scott Wayne, at Dan's farewell party, February 7, 2013

Ray Stata, Dan Sheingold, and Dave Kress at Dan's farewell party.

Dan Sheingold, Ray Stata, and Scott Wayne.

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