

Automated Calibration Technique Reduces DAC Offset to Less than 1 mV

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The transfer function for an N -bit bipolar digital-to-analog converter (DAC) is

$$A = \left(\frac{D}{2^{N-1}} \times G \times V_{FS} \right) - V_{FS} + V_{OS},$$

where A is the analog output, D is the digital input, G is the gain, V_{FS} is the nominal full-scale voltage, and V_{OS} is the offset voltage. For an ideal DAC, $G = 1$ and $V_{OS} = 0$.

The offset error specification, combined with the system requirements, will determine if calibration is needed. The [AD5360](#) 16-bit, 16-channel DAC is factory trimmed, but an offset of several millivolts can still exist. The following example shows how a simple software algorithm can reduce an unknown offset to less than 1 mV (typical). This technique can be used for factory calibration, or for offset correction at any point in the DAC's life cycle.

The AD5360's Offset DAC is used to set the output range, which can be unipolar positive, unipolar negative, bipolar centered, or bipolar skewed. The default value of the Offset DAC sets a ± 10 -V output range when a 5-V reference is used. The Offset DAC also has an offset error. The sixteen DAC outputs are factory trimmed with the Offset DAC at its default value, so this error is trimmed out. As the Offset DAC is changed, its offset error affects the offset errors of the main DAC outputs.

Two features of the AD5360 simplify offset calibration: a GPIO pin, which can have its status determined by reading a register; and an integrated monitor multiplexer, which allows any of the 16 DAC outputs or two external voltages to be switched to a single pin under software control.

Theory of Operation

The offset calibration procedure is as follows: A comparator monitors two voltages, MON_OUT, the DAC output containing an unknown offset; and SIGGND, the ground reference for the DACs. The comparator output indicates whether the unknown offset is above or below SIGGND. The output of the DAC is incremented or decremented until the comparator output toggles, indicating that the DAC output is as close to SIGGND as the comparator can detect. The comparator output is connected to the GPIO pin; its status can be determined by reading the appropriate register. Figure 1 shows the circuit diagram.

The AD5360's multiplexer connects the selected DAC output to MON_OUT. Its switches have a low but finite $R_{DS(on)}$, so any current drawn from MON_OUT creates a voltage drop across R_{DS} , and hence an output error. To prevent this, MON_OUT is buffered by an [AD8597](#) low-noise amplifier. The low pass filter following the amplifier reduces the amount of noise seen by the [AD790](#) fast, precision comparator and prevents false triggering. The AD790 can be operated from ± 15 V supplies, making it compatible with the AD5360. In addition, the AD790 has a 15-V maximum differential input voltage, so it can tolerate the output voltages from the AD5360 without attenuation. In Figure 1, the comparator output will be low if the channel offset is positive, indicating that the output voltage needs to be reduced to remove the offset. The comparator output will be high if the channel offset is negative, indicating that the output voltage needs to be increased to remove the offset.

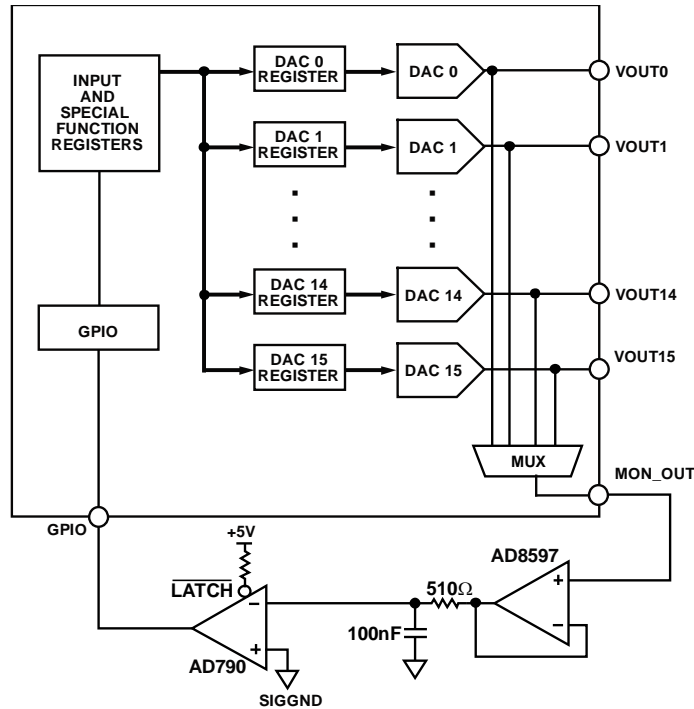


Figure 1. Circuit Diagram

Configuring the Monitor Multiplexer and GPIO of the AD5360.

Writing $0x0C002X$, where X is the required output channel, to the Monitor Special Function Register enables the monitor multiplexer and selects the required channel. When this is done, MON_OUT will give the same output voltage as the selected channel. Bit 0 of the GPIO Special Function Register indicates the status of the GPIO pin. Consult the AD5360 data sheet for information on reading and writing registers.

Calibrating a Channel

Figure 2 shows the calibration routine. The DAC channel is loaded with $0x8000$, which should ideally provide a voltage equal to $SIGGND$ (i.e., 0 V). In this example the DAC channel is assumed to have a negative offset. Reading the GPIO register shows that the comparator output is low, indicating that the input must be incremented until the output toggles. As progressively higher codes are written to the DAC input register, the GPIO register is read until the comparator toggles. Figure 2 shows that this happens at code $0x8009$. The AD790 has a maximum hysteresis band of 0.65 mV , so reducing the DAC code again allows a more accurate determination of the DAC offset. The comparator output toggles again at code $0x8006$. The value that puts the output closest to $SIGGND$ thus lies somewhere between codes $0x8006$ and $0x8009$. In this example, code $0x8007$ is the better choice, but there is no way to determine which code will give the best output using this system. The comparator and op-amp offsets make it impossible to determine which code within the two comparator trip points gives the best result, but in either case the DAC channel is typically $<1\text{ mV}$ from $SIGGND$.

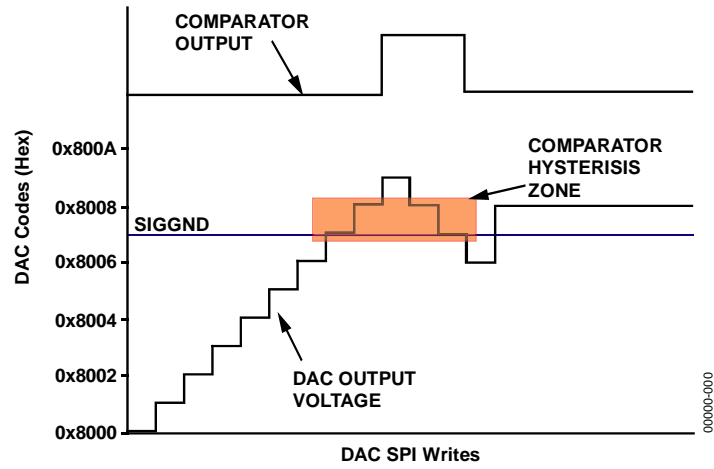


Figure 2. Calibration Routine

Conclusion

This technique makes it possible to reduce an unknown offset error to less than 1 mV using a software algorithm and a few external components.