AN-698
APPLICATION NOTE

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Configuration Registers of the ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ ADM1067/ADM1166

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INTRODUCTION

The ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 family of fully programmable supply sequencers and supervisors can be used as complete supply management solutions in systems using multiple voltage supplies. Such applications include line cards in telecommunications infrastructure equipment (central office, base stations) and blade cards in servers.

All features of the ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 are programmable through an SMBus interface. The devices also contain nonvolatile memory (EEPROM) so that the configuration of these features can be stored on-chip and downloaded on each power-up.

This application note briefly outlines the functions of the devices and provides details of the registers required to set up device configuration.

For more information on the features and functions of the ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166, see the relevant data sheets.

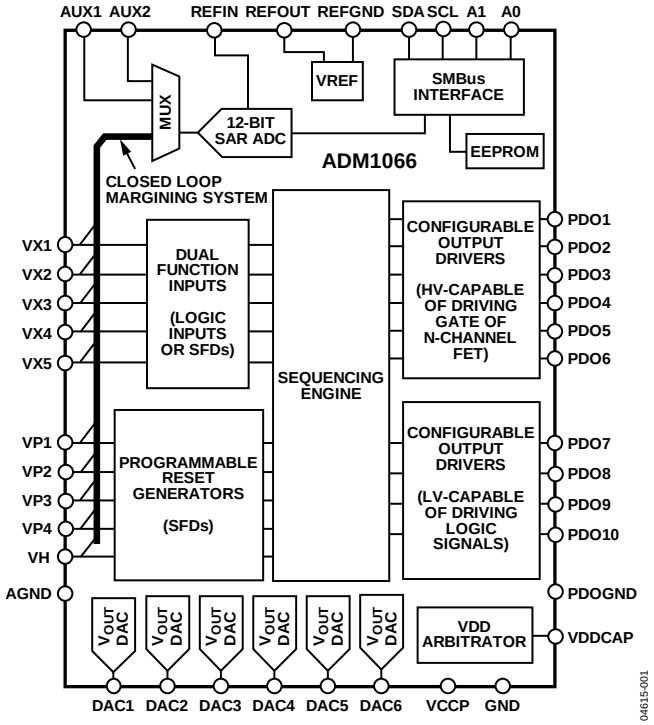

Figure 1. ADM1066 Functional Block Diagram

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REVISION HISTORY

7/13—Rev. B to Rev. C

Changes to Table 3, PDO Status Columns and PDO Pull-Up Columns 13

11/10—Rev. A to Rev. B

Added the ADM1166 ..... Throughout
Changes to Introduction 1
Deleted Figure 2 Through Figure 5 and Figure 7 Through Figure 10 ..... Throughout
Renumbered Figures Sequentially ..... Throughout
Separated Table 6 into Table 6 and Table 7 20
Renumbered Tables Sequentially ..... Throughout
Added Table 9 Through Table 11, Table 20, and Table 21 ..... Throughout
Added the Configuring Sequence Engine States to Write into the Black Box EEPROM on the ADM1166 Section 22
Changes to Table 13 24
Added the Black Box Status Registers and Fault Records on the ADM1166 Section 32
Added the Use of the REVID Section 32
Changes to Table 22 34

2/07—Rev. 0 to Rev. A

UPDATING MEMORY, ENABLING BLOCK ERASE, AND DOWNLOADING EEPROM

This application note contains all of the register information required to configure the many features of the ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166. The devices contain both volatile and nonvolatile memory, which must be set up correctly if any alterations to the configuration are to be updated properly in the device. The volatile memory of the devices is constructed with double buffered latches. For information on this construction, see the relevant device data sheet.

The register/bit map detail in Figure 2 shows the configuration required to

- Update volatile memory in real time.
- Update volatile memory offline, then update all at once.
- Enable block erase.
- Download EEPROM contents to RAM.

There are also a number of configuration bits that are used to update the sequencing engine. These bits are detailed in Table 1

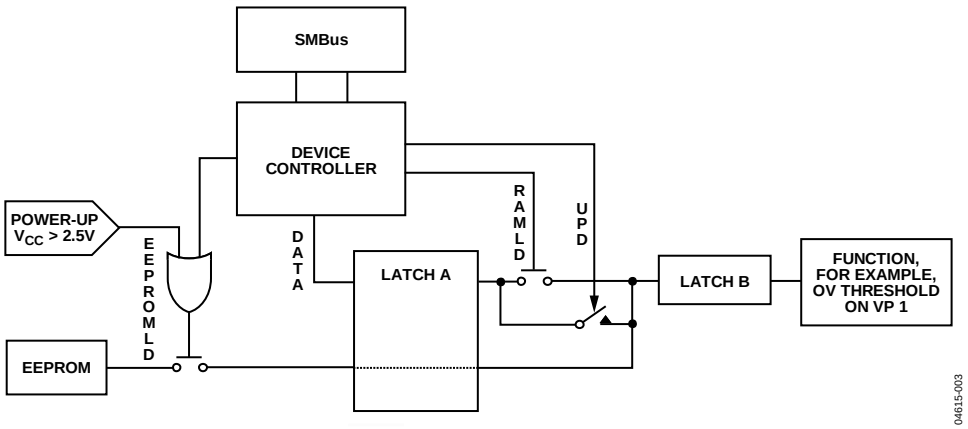

Figure 2. Configuration Update Flow Diagram

Table 1.

Reg.	Reg. Name	Bit No.	Mnemonic	R/W	Description
0x90	UPDCFG	7:3	N/A		Cannot be used.
		2	EEBLKERS	R/W	Enable configuration EEPROM block erase.
		1	CFGUPD	W	Update configuration registers from holding registers (self-clears).
		0	CONTUPD	R/W	Enable continuous update of configuration registers.
0xD8	UDOWNLD	7:1	N/A		Cannot be used.
		0	EEDWNLD	W	Download configuration data from EEPROM. This also happens automatically at power-up. Self-clears on completion.
0xF4	MANID	7:0	MANID	R	Manufacturer's ID, returns 0x41. Can be used to verify communication with the device.

INPUTS

The ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 devices have 10 inputs. Five of these are dedicated supply fault detectors, highly programmable reset generators whose inputs can detect overvoltage, undervoltage, or out-of-window faults. With these five inputs, voltages from 0.573 V to 14.4 V can be supervised. The undervoltage and overvoltage thresholds can all be programmed to an 8-bit resolution. The comparators used to detect faults on the inputs have digitally programmable hysteresis to provide immunity to supply bounce. Each of these inputs also has a glitch filter whose timeout is programmable up to 100 µs.

The other five inputs have dual functionality. They can be used as analog inputs, like the first five channels described earlier in this section, or as general-purpose logic inputs. As analog inputs, these channels function exactly the same as those described earlier in this section. The major difference is that these inputs do not have internal potentiometer resistors and present a true high impedance to the input pin. Their input range is thus limited to 0.573 V to 1.375 V, but the high impedance means that an external resistor divide network can be used to divide down any out-of-range supply to a value within range. Thus, +48 V, +24 V, −5 V, and −12 V can all be supervised by these channels with the appropriate external resistor divide network.

As digital inputs, these pins can be used to detect enable signals (such as PWRGD and POWRON) and are TTL and CMOS compatible. When used in this mode, the analog circuitry of these pins can be mapped to their sister input pins (one of the first five inputs previously described). Thus, VX1 can be used as a second detector on VP1, VX2 can be used with VP2, and so on. VX5 is mapped to VH. With a second detector available, the user can program warnings as well as fault functions.

Table 2 details all of the registers used to configure the inputs to perform the functions described in this section.

Table 2. Registers Used to Configure Inputs

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description			
VP1	0x00	PS1OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on PS1 SFD.			
	0x01	PS1OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS1OVTH when OV is true.			
	0x02	PS1UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on PS1 SFD.			
	0x03	PS1UVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0		5-bit hysteresis to be added from PS1UVTH when UV is true.			
	0x04	SFDV1CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x05	SFDV1SEL	7:2			Cannot be used.			
			1:0	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Select**	
						0	0	Midrange (2.5 V to 6 V)	
						0	1	Low range (1.25 V to 3 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	
VP2	0x08	PS2OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on PS2 SFD.			
	0x09	PS2OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS2OVTH when OV is true.			
	0x0A	PS2UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on PS2 SFD.			
	0x0B	PS2UVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0		5-bit hysteresis to be added from PS2UVTH when UV is true.			
	0x0C	SFDV2CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x0D	SFDV2SEL	7:2			Cannot be used.			
			1:0	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Select**	
						0	0	Mid range (2.5 V to 6 V)	
						0	1	Low range (1.25 V to 3 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description			
VP3	0x10	PS3OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on PS3 SFD.			
	0x11	PS3OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS3OVTH when OV is true.			
	0x12	PS3UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on PS3 SFD.			
	0x13	PS3UVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0		5-bit hysteresis to be added from PS3UVTH when UV is true.			
	0x14	SFDV3CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x15	SFDV3SEL	7:2			Cannot be used.			
			1:0	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Select**	
						0	0	Midrange (2.5 V to 6 V)	
						0	1	Low range (1.25 V to 3 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	
VP4	0x18	PS4OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on PS4 SFD.			
	0x19	PS4OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PS4OVTH when OV is true.			
	0x1A	PS4UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on PS4 SFD.			
	0x1B	PS4UVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0		5-bit hysteresis to be added from PS4UVTH when UV is true.			
	0x1C	SFDV4CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x1D	SFDV4SEL	7:2			Cannot be used.			
			1:0	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Range Select**	
						0	0	Midrange (2.5 V to 6 V)	
						0	1	Low range (1.25 V to 3 V)	
						1	0	Ultralow range (0.573 V to 1.375 V)	
						1	1	Ultralow range (0.573 V to 1.375 V)	

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description			
VH	0x20	PSVHOVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on PSVH SFD.			
	0x21	PSVHOVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from PSVHOVTH when OV is true.			
	0x22	PSVHUVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on PSVH SFD.			
			4:0	HY4 to HY0		5-bit hysteresis to be added from PSVHUVTH when UV is true.			
	0x24	SFDVHCFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x25	SFDVHSEL	7:1			Cannot be used.			
			0	SEL0	R/W	**SEL0**	**Range Select**		
						0	Low range (2.5 V to 6.0 V)		
						1	High range (6.0 V to 14.4 V)		
VX1	0x28	X1OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on X1 SFD.			
	0x29	X1OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X1OVTH when OV is true.			
	0x2A	X1UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on X1 SFD.			
	0x2B	X1UVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0		5-bit hysteresis to be added from X1UVTH when UV is true.			
	0x2C	SFDX1CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x2D	SFDVX1SEL	7:2			Cannot be used.			
			1:0	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Function Select**	
						0	0	SFD (fault) only	
						0	1	GPI (fault) only	
						1	0	GPI (fault) + SFD (warning)	
						1	1	No function (input can still be used as ADC input)	
	0x2E	GPIX1CFG	7			Cannot be used.			
			6	INVIN	R/W	If high, invert input.			
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.			
						INTYP	**Level/Edge**		
						0	Detect level		
						1	Detect edge		

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge has been detected on input.

PULS1	PULS0	Pulse Length (µs)
0	0	10
0	1	100
1	0	1000
1	1	10,000

			2:0	GF2 to GF0	R/W	Glitch filter. Length of time for which a pulse is ignored.

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

VX2	0x30	X2OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on X2 SFD.
	0x31	X2OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X2OVTH when OV is true.
	0x32	X2UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on X2 SFD.
	0x33	X2UVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0		5-bit hysteresis to be added from X2UVTH when UV is true.
	0x34	SFDX2CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	

GF2	GF1	GF0	Delay (µs)
0	0	0	0
0	0	1	5
0	1	0	10
0	1	1	20
1	0	0	30
1	0	1	50
1	1	0	75
1	1	1	100

			1:0	RS1 to RS0	R/W	

RS1	RS0	Fault Type Select
0	0	OV
0	1	UV or OV
1	0	UV
1	1	Off

	0x35	SFDVX2SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	

SEL1	SEL0	Function Select
0	0	SFD (fault) only
0	1	GPI (fault) only
1	0	GPI (fault) + SFD (warning)
1	1	No function (input can still be used as ADC input)

	0x36	GPIX2CFG	7			Cannot be used.
			6	INVIN	R/W	If high, invert input.
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.

INTYP	Level/Edge
0	Detect level
1	Detect edge

			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge has been detected on input.

PULS1	PULS0	Pulse Length (µs)
0	0	10
0	1	100
1	0	1000
1	1	10,000

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description			
			2:0	GF2 to GF0	R/W	Glitch filter. Length of time for which a pulse is ignored.			
						GF2	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
VX3	0x38	X3OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on X3 SFD.			
	0x39	X3OVHYST	7:5			Cannot be used.			
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X3OVTH when OV is true.			
	0x3A	X3UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on X3 SFD.			
	0x3B	X3UVHYST 7	7:5			Cannot be used.			
			4:0	HY4 to HY0		5-bit hysteresis to be added from X3UVTH when UV is true.			
	0x3C	SFDX3CFG	7:5			Cannot be used.			
			4:2	GF2 to GF0	R/W	**GF2**	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100
			1:0	RS1 to RS0	R/W	**RS1**	**RS0**	**Fault Type Select**	
						0	0	OV	
						0	1	UV or OV	
						1	0	UV	
						1	1	Off	
	0x3D	SFDVX3SEL	7:2			Cannot be used.			
			1:0	SEL1 to SEL0	R/W	**SEL1**	**SEL0**	**Function Select**	
						0	0	SFD (fault) only	
						0	1	GPI (fault) only	
						1	0	GPI (fault) + SFD (warning)	
	0x3E	GPIX3CFG	7			Cannot be used.			
			6	INVIN	R/W	If high, invert input.			
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.			
						INTYP Level/Edge			
						0	Detect level		
						1	Detect edge		
			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge has been detected on input.			
						PULS1	**PULS0**	**Pulse Length (µs)**	
						0	0	10	
						0	1	100	
						1	0	1000	
						1	1	10000	
			2:0	GF2 to GF0	R/W	Glitch filter. Length of time for which a pulse is ignored.			
						GF2	**GF1**	**GF0**	**Delay (µs)**
						0	0	0	0
						0	0	1	5
						0	1	0	10
						0	1	1	20
						1	0	0	30
						1	0	1	50
						1	1	0	75
						1	1	1	100

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VX4	0x40	X4OVTH	7:0	OV7 to OVO	R/W	8-bit digital value for the OV threshold on X4 SFD.
	0x41	X4OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X4OVTH when OV is true.
	0x42	X4UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on X4 SFD.
	0x43	X4UVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0		5-bit hysteresis to be added from X4UVTH when UV is true.
	0x44	SFDX4CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)**: 0/0/0/0; 0/0/1/5; 0/1/0/10; 0/1/1/20; 1/0/0/30; 1/0/1/50; 1/1/0/75; 1/1/1/100
			1:0	RS1 to RS0	R/W	**RS1** / **RS0** / **Fault Type Select**: 0/0/OV; 0/1/UV or OV; 1/0/UV; 1/1/Off
	0x45	SFDVX4SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Function Select**: 0/0/SFD (fault) only; 0/1/GPI (fault) only; 1/0/GPI (fault) + SFD (warning); 1/1/No function (input can still be used as ADC input)
	0x46	GPIX4CFG	7			Cannot be used.
			6	INVIN	R/W	If high, invert input.
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.
						INTYP Level/Edge: 0/Detect level; 1/Detect edge
			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge has been detected on input.
						PULS1 / **PULS0** / **Pulse Length (µs)**: 0/0/0; 0/1/100; 1/0/1000; 1/1/10000
			2:0	GF2–GF0	R/W	Glitch filter. Length of time for which a pulse is ignored.
						GF2 / **GF1** / **GF0** / **Delay (µs)**: 0/0/0/0; 0/0/1/5; 0/1/0/10; 0/1/1/20; 1/0/0/30; 1/0/1/50; 1/1/0/75; 1/1/1/100

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VX5	0x48	X5OVTH	7:0	OV7 to OV0	R/W	8-bit digital value for the OV threshold on X5 SFD.
	0x49	5OVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0	R/W	5-bit hysteresis to be subtracted from X5OVTH when OV is true.
	0x4A	X5UVTH	7:0	UV7 to UV0	R/W	8-bit digital value for the UV threshold on X5 SFD.
	0x4B	X5UVHYST	7:5			Cannot be used.
			4:0	HY4 to HY0		5-bit hysteresis to be added from X5UVTH when UV is true.
	0x4C	SFDX5CFG	7:5			Cannot be used.
			4:2	GF2 to GF0	R/W	**GF2** / **GF1** / **GF0** / **Delay (µs)**: 0 0 0 0; 0 0 1 5; 0 1 0 10; 0 1 1 20; 1 0 0 30; 1 0 1 50; 1 1 0 75; 1 1 1 100
			1:0	RS1 to RS0	R/W	**RS1** / **RS0** / **Fault Type Select**: 0 0 OV; 0 1 UV or OV; 1 0 UV; 1 1 Off
	0x4D	SFDVX5SEL	7:2			Cannot be used.
			1:0	SEL1 to SEL0	R/W	**SEL1** / **SEL0** / **Function Select**: 0 0 SFD (fault) only; 0 1 GPI (fault) only; 1 0 GPI (fault) + SFD (warning); 1 1 No function (input can still be used as ADC input)
	0x4E	GPIX5CFG	7			Cannot be used.
			6	INVIN	R/W	If high, invert input.
			5	INTYP	R/W	Determines whether a level or an edge is detected on the pin.
						INTYP Level/Edge: 0 Detect level; 1 Detect edge
			4:3	PULS1 to PULS0	R/W	Length of pulse output once an edge has been detected on input.
						PULS1 / **PULS0** / **Pulse Length (µs)**: 0 0 0; 0 1 100; 1 0 1000; 1 1 10000
			2:0	GF2 to GF0	R/W	Glitch filter. Length of time for which a pulse is ignored.
						GF2 / **GF1** / **GF0** / **Delay (µs)**: 0 0 0 0; 0 0 1 5; 0 1 0 10; 0 1 1 20; 1 0 0 30; 1 0 1 50; 1 1 0 75; 1 1 1 100

OUTPUTS

The ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 devices have 10 programmable driver outputs. Supply sequencing is achieved with the devices by using the PDOx pins as control signals for supplies. The output drivers can be used either as logic enables or FET drivers.

The PDOx pins can be used for a number of functions; the primary function is to provide enable signals for LDOs or dc-to-dc converters, which generate supplies locally on a board. The PDOx can also be used to provide a POWER_GOOD signal when all of the SFDs are in tolerance or to provide a reset output if one of the SFDs goes out of spec (this can be used as a status signal for a DSP, FPGA, or other microcontroller).

The PDOs can be programmed to pull up to a number of different options. The outputs can be programmed as

- Open drain (allowing the user to connect an external pull-up resistor)
- Open drain, with weak pull-up to VDDCAP
- Push-pull to VDDCAP
- Open drain, with weak pull-up to VPx
- Push-pull to VPx
- Strong pull-down to GND
- Internally charge-pumped high drive (12 V, PDO1 to PDO6)

The last option (available only on PDO1 to PDO6) allows the user to directly drive a voltage high enough to fully enhance an external N-FET, which is used to isolate, for example, a card-side voltage from a backplane supply (a PDO sustains greater than 10.5 V into a 1 μA load). The pull-down switches can be used to drive status LEDs.

The data driving each of the PDOx can come from one of three sources. The source can be enabled for a particular output, that is, PDO1, in the PDOCFG configuration register. The data sources are

- An output from the SE.
- Directly from the SMBus. A PDO can be configured so that the SMBus has direct control over it. This enables software control of the PDOs. Thus, a microcontroller can be used to initiate a software power-up/power-down sequence.
- An on-chip clock. A 100 kHz clock is generated on the device. This clock can be made available on any of the PDOs. It could be used to clock an external device such as an LED, for example.

Table 3 details all of the registers used to configure the outputs to perform the functions described in this section.

Table 3. Registers Used to Configure Outputs

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
PDO1	0x07	PDO1CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.
						CFG6 / **CFG5** / **CFG4** / **PDO Status** 0 / 0 / 0 / Disabled, with weak pull-down 0 / 0 / 1 / Enabled, follows the logic driven by the SE 0 / 1 / 0 / Enables SMBus data, drive low 0 / 1 / 1 / Enables SMBus data, drive high 1 / X / X / Enables 100 kHz clock out onto pin
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.
						CFG3 / **CFG2** / **CFG1** / **CFG0** / **PDO Pull-Up** 0 / 0 / 0 / X / None 0 / 0 / 1 / X / Pull-up to 12 V charge pump voltage 0 / 1 / 0 / 0 / Weak open-drain pull-up to VP1 0 / 1 / 0 / 1 / Push-pull pull-up to VP1 0 / 1 / 1 / 0 / Weak open-drain pull-up to VP2 0 / 1 / 1 / 1 / Push-pull pull-up to VP2 1 / 0 / 0 / 0 / Weak open-drain pull-up to VP3 1 / 0 / 0 / 1 / Push-pull pull-up to VP3 1 / 0 / 1 / 0 / Weak open-drain pull-up to VP4 1 / 0 / 1 / 1 / Push-pull pull-up to VP4 1 / 1 / 1 / 0 / Weak open-drain pull-up to VDDCAP 1 / 1 / 1 / 1 / Push-pull pull-up to VDDCAP
PDO2	0x0F	PDO2CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.
						CFG6 / **CFG5** / **CFG4** / **PDO Status** 0 / 0 / 0 / Disabled, with weak pull-down 0 / 0 / 1 / Enabled, follows the logic driven by the SE 0 / 1 / 0 / Enables SMBus data, drive low 0 / 1 / 1 / Enables SMBus data, drive high 1 / X / X / Enables 100 kHz clock out onto pin
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.
						CFG3 / **CFG2** / **CFG1** / **CFG0** / **PDO Pull-Up** 0 / 0 / 0 / X / None 0 / 0 / 1 / X / Pull-up to 12 V charge pump voltage 0 / 1 / 0 / 0 / Weak open-drain pull-up to VP1 0 / 1 / 0 / 1 / Push-pull pull-up to VP1 0 / 1 / 1 / 0 / Weak open-drain pull-up to VP2 0 / 1 / 1 / 1 / Push-pull pull-up to VP2 1 / 0 / 0 / 0 / Weak open-drain pull-up to VP3 1 / 0 / 0 / 1 / Push-pull pull-up to VP3 1 / 0 / 1 / 0 / Weak open-drain pull-up to VP4 1 / 0 / 1 / 1 / Push-pull pull-up to VP4 1 / 1 / 1 / 0 / Weak open-drain pull-up to VDDCAP 1 / 1 / 1 / 1 / Push-pull pull-up to VDDCAP
PDO3	0x17	PDO3CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.
						CFG6 / **CFG5** / **CFG4** / **PDO Status** 0 / 0 / 0 / Disabled, with weak pull-down 0 / 0 / 1 / Enabled, follows the logic driven by the SE 0 / 1 / 0 / Enables SMBus data, drive low 0 / 1 / 1 / Enables SMBus data, drive high 1 / X / X / Enables 100 kHz clock out onto pin

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
PDO4	0x1F	PDO4CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak open-drain pull-up to VDDCAP

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
PDO5	0x27	PDO5CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak open-drain pull-up to VDDCAP

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
PDO6	0x2F	PDO6CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Pull-up to 12 V charge pump voltage
0	1	0	0	Weak open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

PDO7	0x37	PDO7CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Do not use
0	1	0	0	Weak open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

PDO8	0x3F	PDO8CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Do not use
0	1	0	0	Weak open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
PDO9	0x47	PDO9CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.

CFG3	CFG2	CFG1	CFG0	PDO Pull-Up
0	0	0	X	None
0	0	1	X	Do not use
0	1	0	0	Weak open-drain pull-up to VP1
0	1	0	1	Push-pull pull-up to VP1
0	1	1	0	Weak open-drain pull-up to VP2
0	1	1	1	Push-pull pull-up to VP2
1	0	0	0	Weak open-drain pull-up to VP3
1	0	0	1	Push-pull pull-up to VP3
1	0	1	0	Weak open-drain pull-up to VP4
1	0	1	1	Push-pull pull-up to VP4
1	1	1	0	Weak open-drain pull-up to VDDCAP
1	1	1	1	Push-pull pull-up to VDDCAP

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
PDO10	0x4F	PDO10CFG	7			Cannot be used.
			6:4	CFG6 to CFG4	R/W	Controls the logic source driving the PDO, that is, the SE, the internal clock, or the SMBus, directly.

CFG6	CFG5	CFG4	PDO Status
0	0	0	Disabled, with weak pull-down
0	0	1	Enabled, follows the logic driven by the SE
0	1	0	Enables SMBus data, drive low
0	1	1	Enables SMBus data, drive high
1	X	X	Enables 100 kHz clock out onto pin

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description				
			3:0	CFG3 to CFG0	R/W	Determines the format of the pull-up on the PDO.				
						CFG3	**CFG2**	**CFG1**	**CFG0**	**PDO Pull-Up**
						0	0	0	X	None
						0	0	1	X	Do not use
						0	1	0	0	Weak open-drain pull-up to VP1
						0	1	0	1	Push-pull pull-up to VP1
						0	1	1	0	Weak open-drain pull-up to VP2
						0	1	1	1	Push-pull pull-up to VP2
						1	0	0	0	Weak open-drain pull-up to VP3
						1	0	0	1	Push-pull pull-up to VP3
						1	0	1	0	Weak open-drain pull-up to VP4
						1	0	1	1	Push-pull pull-up to VP4
						1	1	1	0	Weak open-drain pull-up to VDDCAP
						1	1	1	1	Push-pull pull-up to VDDCAP

SEQUENCING ENGINE

The ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 incorporate a sequencing engine (SE) that provides the user with powerful and flexible control of sequencing. The SE implements state machine control of the PDO outputs, with state changes conditional on input events. SE programs can enable complex control of boards, such as power-up and power-down sequence control, fault event handling, and interrupt generation on warnings. A watchdog function to verify the continued operation of a processor clock can be integrated into the SE program. The SE can also be controlled via the SMBus, giving software or firmware control of the board sequencing.

Considering the function of the SE from an applications viewpoint, it is best to think of the SE as providing a state for a state machine. This state has the following attributes:

- It is used to monitor signals indicating the status of the 10 input pins, VP1 to VP4, VH, and VX1 to VX5.
- It can be entered from any other state.
- There are three exit routes that move the state machine to the next state: end-of-step detection, monitoring fault, and timeout.
- Delay timers for the end-of-step and timeout blocks can be programmed independently and change with each state change. The range of timeouts is from 0 ms to 400 ms.
- The output condition of the 10 PDO pins is defined and fixed within a state.
- The transition from one state to the next is made in less than 20 µs, the time taken to download a state definition from EEPROM to the SE.

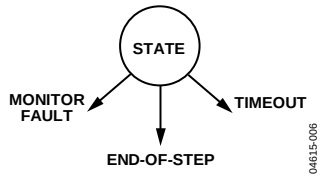

Figure 3. State Cell

The ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 offer up to 63 such state definitions. Each state is defined by a 64-bit word.

Table 4 shows the details of the 64 bits that define a state. Table 8 details how to communicate with the SE in the ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166. Table 9 provides details of additional sequence engine control registers present in the ADM1166 that allow the sequence engine to be restarted.

Table 4. Starting Address for Each State in SE

State	Start Address	State	Start Address
Reserved State	FA00	State 32	FB00
State 1	FA08	State 33	FB08
State 2	FA10	State 34	FB10
State 3	FA18	State 35	FB18
State 4	FA20	State 36	FB20
State 5	FA28	State 37	FB28
State 6	FA30	State 38	FB30
State 7	FA38	State 39	FB38
State 8	FA40	State 40	FB40
State 9	FA48	State 41	FB48
State 10	FA50	State 42	FB50
State 11	FA58	State 43	FB58
State 12	FA60	State 44	FB60
State 13	FA68	State 45	FB68
State 14	FA70	State 46	FB70
State 15	FA78	State 47	FB78
State 16	FA80	State 48	FB80
State 17	FA88	State 49	FB88
State 18	FA90	State 50	FB90
State 19	FA98	State 51	FB98
State 20	FAA0	State 52	FBA0
State 21	FAA8	State 53	FBA8
State 22	FAB0	State 54	FBB0
State 23	FAB8	State 55	FBB8
State 24	FAC0	State 56	FBC0
State 25	FAC8	State 57	FBC8
State 26	FAD0	State 58	FBD0
State 27	FAD8	State 59	FBD8
State 28	FAE0	State 60	FBE0
State 29	FAE8	State 61	FBE8
State 30	FAF0	State 62	FBF0
State 31	FAF8	State 63	FBF8

Table 5. Bitmap for Definition of Each State in SE

Bit No.	Operation, or If Set to 0	If Set to 1	Description
0	PDO1 output data		
1	PDO2 output data		
2	PDO3 output data		
3	PDO4 output data		
4	PDO5 output data		
5	PDO6 output data		
6	PDO7 output data		
7	PDO8 output data		
8	PDO9 output data		
9	PDO10 output data		
10	Monitor fault if VP1 = 0	Monitor fault if VP1 = 1	Monitoring of faults on VP1 must be unmasked for this function to execute (next bit).
11	Mask VP1 monitoring	Unmask VP1 monitoring	Bit 11 = 1; turns on monitoring on the VP1 channel.
12	Monitor fault if VP2 = 0	Monitor fault if VP2 = 1	Monitoring of faults on VP2 must be unmasked for this function to execute (next bit).
13	Mask VP2 monitoring	Unmask VP2 monitoring	Bit 13 = 1; turns on monitoring on the VP2 channel.
14	Monitor Fault if VP3 = 0	Monitor fault if VP3 = 1	Monitoring of faults on VP3 must be unmasked for this function to execute (next bit).
15	Mask VP3 monitoring	Unmask VP3 monitoring	Bit 15 = 1; turns on monitoring on the VP3 channel.
16	Monitor fault if VP4 = 0	Monitor fault if VP4 = 1	Monitoring of faults on VP4 must be unmasked for this function to execute (next bit).
17	Mask VP4 monitoring	Unmask VP4 monitoring	Bit 17 = 1; turns on monitoring on the VP4 channel.
18	Monitor fault if VH = 0	Monitor fault if VH = 1	Monitoring of faults on VH must be unmasked for this function to execute (next bit).
19	Mask VH monitoring	Unmask VH monitoring	Bit 19 = 1; turns on monitoring on the VH channel.
20	Monitor fault if VX1 = 0	Monitor fault if VX1 = 1	Monitoring of faults on VX1 must be unmasked for this function to execute (next bit).
21	Mask VX1 monitoring	Unmask VX1 monitoring	Bit 21 = 1; turns on monitoring on the VX1 channel.
22	Monitor fault if VX2 = 0	Monitor fault if VX2 = 1	Monitoring of faults on VX2 must be unmasked for this function to execute (next bit).
23	Mask VX2 monitoring	Unmask VX2 monitoring	Bit 23 = 1; turns on monitoring on the VX2 channel.
24	Monitor fault if VX3 = 0	Monitor fault if VX3 = 1	Monitoring of faults on VX3 must be unmasked for this function to execute (next bit).
25	Mask VX3 monitoring	Unmask VX3 monitoring	Bit 25 = 1; turns on monitoring on the VX3 channel.
26	Monitor fault if VX4 = 0	Monitor fault if VX4 = 1	Monitoring of faults on VX4 must be unmasked for this function to execute (next bit).
27	Mask VX4 monitoring	Unmask VX4 monitoring	Bit 27 = 1; turns on monitoring on the VX4 channel.
28	Monitor fault if VX5 = 0	Monitor fault if VX5 = 1	Monitoring of faults on VX5 must be unmasked for this function to execute (next bit).
29	Mask VX5 monitoring	Unmask VX5 monitoring	Bit 29 = 1; turns on monitoring on the VX5 channel.
30	Mask WARNING monitoring	Unmask WARNING monitoring	Can only generate a monitor fault on WARNING = 1. Is unmasked.
31	TIMEOUT<0>		Timeout length (see Table 6).
32	TIMEOUT<1>		
33	TIMEOUT<2>		
34	TIMEOUT<3>		
35	SEQCOND<0>		Sequence condition (see Table 6).
36	SEQCOND<1>		
37	SEQCOND<2>		
38	SEQCOND<3>		
39	Sequence on selected input = high	Sequence on selected input = low	SEQSENSE
40	SEQDELAY<0>		Sequence delay (see Table 6).
41	SEQDELAY<1>		
42	SEQDELAY<2>		

Bit No.	Operation, or If Set to 0	If Set to 1	Description
43	SEQDELAY<3>		
44	MONADDR<0>		MONADDR<5:0> is the state number to jump to if a monitor function fault occurs.
45	MONADDR<1>		
46	MONADDR<2>		
47	MONADDR<3>		
48	MONADDR<4>		
49	MONADDR<5>		
50	TIMADDR<0>		TIMADDR<5:0> is the state number to jump to if a timeout fault occurs.
51	TIMADDR<1>		
52	TIMADDR<2>		
53	TIMADDR<3>		
54	TIMADDR<4>		
55	TIMADDR<5>		
56	SEQADDR<0>		SEQADDR<5:0> is the state number to jump to if a sequence fault occurs.
57	SEQADDR<1>		
58	SEQADDR<2>		
59	SEQADDR<3>		
60	SEQADDR<4>		
61	SEQADDR<5>		
62	Round robin disable	Round robin enable	This is OR'ed with enable (Address 0x82[1]).
63	Fault latch closed	Fault latch open	

Table 6. Timeouts and Delays for Functions in the SE

TIMEOUT<3:0>	SEQDELAY<3:0>Delay (ms)
0	Cannot be used
1	0.1
2	0.2
3	0.4
4	0.7
5	1
6	2
7	4
8	7
9	10
10	20
11	40
12	70
13	100
14	200
15	400

Table 7. SEQCOND and Sequence on Signal From in the SE

SEQCOND<3:0>	Sequence On Signal From
0	Never sequence; set SEQSENSE = 0 always to ensure no sequence (Bit 39).
1	VP1.
2	VP2.
3	VP3.
4	VP4.
5	VH.
6	VX1.
7	VX2.
8	VX3.
9	VX4.
10	VX5.
11	WARNING.
12	SMBus jump. Wait for the SMBus command before jumping to the next state. Set SEQSENSE = 0 to ensure proper operation.

Table 8. Communicating with the SE

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x93	SECTRL	7:3	N/A		Cannot be used.
		2	SMBus jump	W	Allows software control of SE state changes. Can force an unconditional jump to the next state. The bit can be set as the condition for an end-of-step change. This enables the user to clear external interrupts by moving forward a state. The bit self-clears to 0 after the state change has occurred.
		1	SWSTEP	R/W	Step the SE forward to the next state. Use in conjunction with the halt bit to step through a sequence. Can be used as a tool for debugging sequences.
		0	Halt	R/W	Halt the SE. State changes will not happen. Must be set to allow read, erase, or write access to the SE EEPROM.
0xE9	SEADDR	7:6	N/A		
		5:0	ADDR	R	SE current state used in conjunction with the halt bit (Address 0x93[0]).

Table 9. Additional ADM1166 Sequence Engine Control Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xDA	UNLOCKSE	7:0	Unlock Key	W	Writing 0x27 and then 0x10 to this register in consecutive writes unlocks the SEDOWNLD register so that it can be written to. To reset the lock, write 0x00 into the unlock key. Writing to SEDOWNLD does not reset the lock.
0xDB	SEDOWNLD	7:1	N/A		Cannot be used.
		0	Restart	W	1 causes the sequence engine to restart from the reserved state.

CONFIGURING SEQUENCE ENGINE STATES TO WRITE INTO THE BLACK BOX EEPROM ON THE ADM1166

The ADM1166 can use a section of EEPROM to store fault records when the sequence engine enters a user defined trigger state. These states are defined in EEPROM and downloaded to registers along with the other configuration data when the ADM1166 is being initialized. The register locations of the black box write triggers are shown in Table 10. These are loaded from the same locations in the 0xF8xx EEPROM block. The BBWRTRGx registers are read/write and, therefore, can be modified by software if required after the download.

When one or more of the bits in the BBWRTRx registers are set to 1, the black box is enabled, and fault records are written into EEPROM when the sequence engine enters a state that has its corresponding BBWRTRGx bit set to 1.

When the black box is enabled, all access to the configuration, user, and black box EEPROM sections is inhibited unless the BBCTRL.HALT bit is written to 1 to stop the black box.

When an ADM1166 powers up, the black box automatically searches the black box section of EEPROM to find the first unused location for the next fault record to be written. After this section of EEPROM is erased, the black box may be instructed to perform this search again so that it uses the correct location for the next fault record write. The BBSEARCH.RESET bit is used to initiate this action.

Table 10. ADM1166 Bitmap for Definition of Black Box Write Triggers for Each SE State[1]

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x94	BBWRTRG1	7	STATE7	R/W	State 7 write trigger.
		6	STATE6	R/W	State 6 write trigger.
		5	STATE5	R/W	State 5 write trigger.
		4	STATE4	R/W	State 4 write trigger.
		3	STATE3	R/W	State 3 write trigger.
		2	STATE2	R/W	State 2 write trigger.
		1	STATE1	R/W	State 1 write trigger.
		0	Reserved	R/W	Reserved state black box trigger; must always be set to 0.
0x95	BBWRTRG2	7	STATE15	R/W	State 15 write trigger.
		6	STATE14	R/W	State 14 write trigger.
		5	STATE13	R/W	State 13 write trigger.
		4	STATE12	R/W	State 12 write trigger.
		3	STATE11	R/W	State 11 write trigger.
		2	STATE10	R/W	State 10 write trigger.
		1	STATE9	R/W	State 9 write trigger.
		0	STATE8	R/W	State 8 write trigger.
0x96	BBWRTRG3	7	STATE23	R/W	State 23 write trigger.
		6	STATE22	R/W	State 22 write trigger.
		5	STATE21	R/W	State 21 write trigger.
		4	STATE20	R/W	State 20 write trigger.
		3	STATE19	R/W	State 19 write trigger.
		2	STATE18	R/W	State 18 write trigger.
		1	STATE17	R/W	State 17 write trigger.
		0	STATE16	R/W	State 16 write trigger.
0x97	BBWRTRG4	7	STATE31	R/W	State 31 write trigger.
		6	STATE30	R/W	State 30 write trigger.
		5	STATE29	R/W	State 29 write trigger.
		4	STATE28	R/W	State 28 write trigger.
		3	STATE27	R/W	State 27 write trigger.
		2	STATE26	R/W	State 26 write trigger.
		1	STATE25	R/W	State 25 write trigger.
		0	STATE24	R/W	State 24 write trigger.
0x98	BBWRTRG5	7	STATE39	R/W	State 39 write trigger.
		6	STATE38	R/W	State 38 write trigger.
		5	STATE37	R/W	State 37 write trigger.
		4	STATE36	R/W	State 36 write trigger.
		3	STATE35	R/W	State 35 write trigger.

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
		2	STATE34	R/W	State 34 write trigger.
		1	STATE33	R/W	State 33 write trigger.
		0	STATE32	R/W	State 32 write trigger.
0x99	BBWRTRG6	7	STATE47	R/W	State 47 write trigger.
		6	STATE46	R/W	State 46 write trigger.
		5	STATE45	R/W	State 45 write trigger.
		4	STATE44	R/W	State 44 write trigger.
		3	STATE43	R/W	State 43 write trigger.
		2	STATE42	R/W	State 42 write trigger.
		1	STATE41	R/W	State 41 write trigger.
		0	STATE40	R/W	State 40 write trigger.
0x9A	BBWRTRG7	7	STATE55	R/W	State 55 write trigger.
		6	STATE54	R/W	State 54 write trigger.
		5	STATE53	R/W	State 53 write trigger.
		4	STATE52	R/W	State 52 write trigger.
		3	STATE51	R/W	State 51 write trigger.
		2	STATE50	R/W	State 50 write trigger.
		1	STATE49	R/W	State 49 write trigger.
		0	STATE48	R/W	State 48 write trigger.
0x9B	BBWRTRG8	7	STATE63	R/W	State 63 write trigger.
		6	STATE62	R/W	State 62 write trigger.
		5	STATE61	R/W	State 61 write trigger.
		4	STATE60	R/W	State 60 write trigger.
		3	STATE59	R/W	State 59 write trigger.
		2	STATE58	R/W	State 58 write trigger.
		1	STATE57	R/W	State 57 write trigger.
		0	STATE56	R/W	State 56 write trigger.

[1] When the trigger bit for a given state is set to 1, a fault record is written into the next free location in the black box section of EEPROM when the sequence engine enters that state. When the trigger bit is set to 0, no fault record is written.

Table 11. ADM1166 Black Box Control Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x9C	BBCTRL	7:1	N/A		Cannot be used.
		0	HALT	R/W	The black box function is enabled when one or more of the BBWRTRGx register bits are set to 1. When the black box is enabled, it is no longer possible to read or write to the configuration, user, and black box sections of EEPROM. Writing this bit to 1 disables the black box and enables read and write access to the configuration, user, and black box sections of EEPROM. This bit cannot be set while a fault record is being written into the EEPROM; therefore, this bit should always be read after a write to ensure that the bit is set correctly.
0XD9	BBSEARCH	7:1	N/A		Cannot be used.
		0	RESET	R	When written to 1, the black box searches from Address 0xF980 to find the first unused fault record. After erasing the section of EEPROM holding the black box fault records, and for the black box to start writing records from the first location, this bit should be written to 1.

ADM1062/ADM1063/ADM1064/ADM1066/ADM1166 ADC

The ADM1062, ADM1063, ADM1064, ADM1066, and ADM1166 all feature an on-chip 12-bit ADC. The ADC has a 12-channel (13-channel on the ADM1063) analog mux on the front end. Any or all of these inputs can be selected to be read by the ADC. Thus the ADC can be set up to continuously read the selected channels. The circuit controlling this operation is called the round robin (RR). The user selects the channels to operate on, and the ADC performs a conversion on each in turn. Averaging can be turned on, setting the round robin to take 16 conversions on each channel; otherwise, a single conversion is made on each channel. At the end of this cycle, the results are written to the output registers and, at the same time, compared with preset thresholds provided on the ADM1062/ADM1063/ADM1064/ADM1066/ADM1166, which can be programmed to a maximum or minimum allowable threshold. Only one register is provided for each input channel; therefore, a UV or OV threshold, but not both, can be set for a given channel. Exceeding the threshold generates a warning that can be read back from the status registers or input into the SE via an OR gate. The round robin can be enabled via an SMBus write or can be programmed to turn on at a particular point in the SE program; for instance, it can be set to start once a power-up sequence is complete and all supplies are known to be within expected fault limits.

Table 12 through Table 17 show the details of the registers required to set up the ADC and its inputs.

ADC Readback Configuration Registers

Table 12. Limit Registers—An ADC Reading Above or Below This Limit Generates a Warning

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VP1	0x70	ADCVP1LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VP1 input.
VP2	0x71	ADCVP2LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VP2 input.
VP3	0x72	ADCVP3LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VP3 input.
VP4	0x73	ADCVP4LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VP4 input.
VH	0x74	ADCVHLIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VH input.
VX1	0x75	ADCVX1LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX1 input.
VX2	0x76	ADCVX2LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX2 input.
VX3	0x77	ADCVX3LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX3 input.
VX4	0x78	ADCVX4LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on VX4 input.
VX5	0x79	ADCVX5LIM		LIM7 to LIM0	R/W	Limit register for ADC conversion on VX5 input.
INTS	0x7A	ADCITLIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on internal temp sensor (ADM1062, ADM1063 only).
AUX1	0x7A	ADCAUX1LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on the AUX1 channel (ADM1064, ADM1066 only).
EXTS1	0x7B	ADCXTS1LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on External Temp Sensor 1 (ADM1062, ADM1063 only).
AUX2	0x7B	ADCAUX2LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on the AUX2 channel. (ADM1064, ADM1066 only).
EXTS2	0x7C	ADCXTS2LIM	7:0	LIM7 to LIM0	R/W	Limit register for ADC conversion on External Temp Sensor 2 (ADM1063 only).

Table 13. Sense Registers—Determine When a Warning Is Generated

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VX3	0x7D	LSENSE1	7	SENS7	R/W	Limit sense for VX3. (0 = ADC > ADCVX3LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX3LIM gives a warning, that is, undervoltage)
VX2			6	SENS6	R/W	Limit sense for VX2. (0 = ADC > ADCVX2LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX2LIM gives a warning, that is, undervoltage)
VX1			5	SENS5	R/W	Limit sense for VX1. (0 = ADC > ADCVX1LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX1LIM gives a warning, that is, undervoltage)
VH			4	SENS4	R/W	Limit sense for VH. (0 = ADC > ADCVHLIM gives a warning, that is, overvoltage; 1 = ADC < ADCVHLIM gives a warning, that is, undervoltage)
VP4			3	SENS3	R/W	Limit sense for VP4. (0 = ADC > ADCVP4LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVP4LIM gives a warning, that is, undervoltage)
VP3			2	SENS2	R/W	Limit sense for VP3 (0 = ADC > ADCVP3LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVP3LIM gives a warning, that is, undervoltage)

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VP2			1	SENS1	R/W	Limit sense for VP2. (0 = ADC > ADCVP2LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVP2LIM gives a warning, that is, undervoltage)
VP1			0	SENS0	R/W	Limit sense for VP1. (0 = ADC > ADCVP1LIM gives a warning, that is, overvoltage; 1= ADC < ADCVP1LIM gives a warning, that is, undervoltage)
	0x7E	LSENSE2	7	SENS7		Cannot be used.
			6	SENS6		Cannot be used.
			5	SENS5		Cannot be used.
EXTS2			4	SENS4	R/W	Limit sense for External Temp Sensor 2 (ADM1063 only). (0 = ADC > ACXTS2LIM gives a warning, that is, overvoltage; 1 = ADC < ACXTS2LIM gives a warning, that is, undervoltage)
AUX2			3	SENS3	R/W	Limit sense for AUX2 (ADM1064, ADM1066 only). (0 = ADC > ADCAUX2LIM gives a warning, that is, overvoltage; 1 = ADC < ADCAUX2LIM gives a warning, that is, undervoltage)
EXTS1			3	SENS3	R/W	Limit sense for External Temp Sensor 1 (ADM1062, ADM1063 only). (0 = ADC > ACXTS1LIM gives a warning, that is, overvoltage; 1 = ADC < ACXTS1LIM gives a warning, that is, undervoltage)
AUX1			2	SENS2	R/W	Limit sense for AUX1 (ADM1064, ADM1066 only). (0 = ADC > ADCAUX1LIM gives a warning, that is, overvoltage; 1 = ADC < ADCAUX1LIM gives a warning, that is, undervoltage)
INTS			2	SENS2	R/W	Limit sense for internal temp sensor (ADM1062, ADM1063 only). (0 = ADC > ADCITLIM gives a warning, that is, overvoltage; 1 = ADC < ADCITLIM gives a warning, that is, undervoltage)
VX5			1	SENS1	R/W	Limit sense for VX5. (0 = ADC > ADCVX5LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX5LIM gives a warning, that is, undervoltage)
VX4			0	SENS0	R/W	Limit sense for VX4. (0 = ADC > ADCVX4LIM gives a warning, that is, overvoltage; 1 = ADC < ADCVX4LIM gives a warning, that is, undervoltage)

Table 14. Round Robin Select Registers—Determine Which Inputs Are Actually Read by the ADC As It Cycles

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VX3	0x80	RRSEL1	7	VX3CHAN	R/W	0 = VX3 is included in RR. 1 = VX3 is excluded from RR.
VX2			6	VX2CHAN	R/W	0 = VX2 is included in RR. 1 = VX2 is excluded from RR.
VX1			5	VX1CHAN	R/W	0 = VX1 is included in RR. 1 = VX1 is excluded from RR.
VH			4	VHCHAN	R/W	0 = VH is included in RR. 1 = VH is excluded from RR.
VP4			3	VP4CHAN	R/W	0 = VP4 is included in RR. 1 = VP4 is excluded from RR.
VP3			2	VP3CHAN	R/W	0 = VP3 is included in RR. 1 = VP3 is excluded from RR.
VP2			1	VP2CHAN	R/W	0 = VP2 is included in RR. 1 = VP2 is excluded from RR.
VP1			0	VP1CHAN	R/W	0 = VP1 is included in RR. 1 = VP1 is excluded from RR.
	0x81	RRSEL2	7			Cannot be used.
			6			Cannot be used.
			5			Cannot be used.
EXTS2			4	EXTCH2	R/W	0 = External Temp Sensor 2 is included in RR. 1 = External Temp Sensor 2 is excluded from RR (ADM1063 only).
AUX2			3	AUX2CHAN	R/W	0 = Auxiliary Channel 2 is included in RR. 1 = Auxiliary Channel 2 is excluded from RR (ADM1064, ADM1066 only).
EXTS1			3	EXTCH1	R/W	0 = External Temp Sensor 1 is included in RR. 1 = External Temp Sensor 1 is excluded from RR (ADM1062, ADM1063 only).
AUX1			2	AUX1CHAN	R/W	0 = Auxiliary Channel 1 is included in RR. 1 = Auxiliary Channel 1 is excluded from RR (ADM1064, ADM1066 only).
INTS			2	INTSCHAN	R/W	0 = Internal Temp Sensor 1 is included in RR. 1 = Internal Temp Sensor 1 is excluded from RR (ADM1062, ADM1063 only).
VX5			1	VX5CHAN	R/W	0 = VX5 is included in RR. 1= VX5 is excluded from RR.
VX4			0	VX4CHAN	R/W	0 = VX4 is included in RR. 1= VX4 is excluded from RR.

Table 15. Round Robin Control Register—Activates ADC Read and Determines Whether Averaging Is Used and Whether There Is a Continuous Read

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x82	RRCTRL	7:5			Cannot be used.
		4	ClearLIM	R/W	Write this bit high to clear limit warnings. This bit then self-clears.
		3	StopWrite	R/W	Inhibits the RR from writing the results to the output registers.
		2	Average	R/W	Turn on 16× averaging.
		1	Enable	R/W	Turn on the RR for continuous operation.
		0	Go	R/W	Start the RR.

Table 16. Temperature Sensor Configuration Register

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x83	TSCTRL	7:3	N/A		Cannot be used.
		2	LOWDN2	R/W	Turn off VBE biasing for DN2 (ADM1063 only).
		1	LOWDN1	R/W	Turn off VBE biasing for DN1.
		0	DIODE_CK	R/W	Set this bit to perform a diode check. If set, this causes the ADC result for the two external channels to limit at full-scale positive if a diode is present. Used for board checking.

Table 17. ADC Value Registers

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VP1	0xA0	ADCHVP1	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VP1 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VP1 when 0x82[2] (average) = 1.
	0xA1	ADCLVP1	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VP1 input.
VP2	0xA2	ADCHVP2	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VP2 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VP2 when 0x82[2] (average) = 1.
	0xA3	ADCLVP2	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VP2 input.
VP3	0xA4	ADCHVP3	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VP3 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VP3 when 0x82[2] (average) = 1.
	0xA5	ADCLVP3	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VP3 input.
VP4	0xA6	ADCHVP4	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VP4 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VP4 when 0x82[2] (average) = 1.
	0xA7	ADCLVP4	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VP4 input.
VH	0xA8	ADCHVH	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VH when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VH when 0x82[2] (average) = 1.
	0xA9	ADCLVH	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VH input.
VX1	0xAA	ADCHVX1	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX1 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX1 when 0x82[2] (average) = 1.
	0xAB	ADCLVX1	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX1 input.
VX2	0xAC	ADCHVX2	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX2 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX2 when 0x82[2] (average) = 1.
	0xAD	ADCLVX2	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX2 input.
VX3	0xAE	ADCHVX3	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX3 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX3 when 0x82[2] (average) = 1.
	0xAF	ADCLVX3	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX3 input.

Input	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
VX4	0xB0	ADCHVX4	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX4 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX4 when 0x82[2] (average) = 1.
	0xB1	ADCLVX4	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX4 input.
VX5	0xB2	ADCHVX5	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of ADC conversions on VX5 when 0x82[2] (average) = 0.
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of ADC conversions on VX5 when 0x82[2] (average) = 1.
	0xB3	ADCLVX5	7:0	OUT7 to OUT0	R/W	8 LSBs of 12- or 16-bit result of the ADC conversions on VX5 input.
INTS	0xB4	ADCHITS	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of internal temp sensor conversion (ADM1062, ADM1063 only).
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of internal temp sensor conversion (ADM1062, ADM1063 only).
	0xB5	ADCLITS	7:0	OUT7 to OUT0	R/W	Low byte of internal temp sensor conversion (ADM1062, ADM1063 only).
AUX1	0xB4	ADCHAUX1	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of AUX1 conversion (ADM1064, ADM1066 only).
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of AUX1 conversion (ADM1064, ADM1066 only).
	0xB5	ADCLAUX1	7:0	OUT7 to OUT0	R/W	Low byte of AUX1 conversion (ADM1064, ADM1066 only).
EXTS1	0xB6	ADCHXTS1	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of External Temp Sensor 1 conversion (ADM1062, ADM1063 only).
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of External Temp Sensor 1 conversion (ADM1062, ADM1063 only).
	0xB7	ADCLXTS1	7:0	OUT7 to OUT0	R/W	Low byte of External Temp Sensor 1 conversion (ADM1062, ADM1063 only).
AUX2	0xB6	ADCHAUX2	7:4			Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of AUX2 conversion (ADM1064, ADM1066 only).
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of AUX2 conversion (ADM1064, ADM1066 only).
	0xB7	ADCLAUX2	7:0	OUT7 to OUT0	R/W	Low byte of AUX2 conversion (ADM1064, ADM1066 only).
EXTS2	0xB8	ADCHXTS2	7:4	N/A		Not used if 0x82[2] (average) = 0.
			3:0	OUT3 to OUT0	R/W	4 MSBs of 12-bit result of External Temp Sensor 2 conversion (ADM1063 only).
			7:0	OUT7 to OUT0	R/W	8 MSBs of 16-bit result of External Temp Sensor 2 conversion (ADM1063 only).
	0xB9	ADCLXTS2	7:0	OUT7 to OUT0	R/W	Low byte of External Temp Sensor 2 conversion (ADM1063 only).

ADM1062/ADM1066/ADM1067/ADM1166 DACS

The ADM1062, ADM1066, and ADM1067 feature six voltage output DACs. These DACs are primarily used to adjust the output voltage of a dc-to-dc converter by altering the current at its feedback node. These DACs, therefore, provide an open-loop margining system. The ADC on the ADM1062 and ADM1066 closes this loop. For more information on margining, see the relevant data sheets.

When the DACx output buffer is turned on, it has very little effect on the dc-to-dc output. The DAC output buffer has been designed to power up without glitching. It does this by first powering up the buffer to follow the pin voltage and does not drive out onto the pin at this time. Once the output buffer is properly enabled, the buffer input is switched over to the DAC, and the output stage of the buffer is turned on. Output glitching is negligible.

Four DAC ranges are offered, and these are placed with midcode (Code 0x7F) at 0.6 V, 0.8 V, 1.0 V, and 1.25 V to correspond to the most common feedback voltages. Centering the DAC outputs in this way provides the best use of the DAC resolution; that is, for most supplies it is possible to place the DAC midcode at the point where the dc-to-dc output is not modified, thus giving each of the DACs one half of the full range to margin up and down. The DAC output voltage is set by the code written to the DACx register. The voltage is linear with the unsigned binary number in this register. Code 0x7F is placed at the midcode voltage. The output voltage is given by the following equation:

$$DACoutput = (DACx - 0x7F)/255 \times 0.6015 + V_{OFF}$$

where V_{OFF} is one of the four offset voltages described earlier in this section.

Limit registers (called DPLIMx and DNLIMx) on the device offer the user some protection from firmware bugs that can cause catastrophic board problems by forcing supplies beyond their allowable output ranges. Essentially, the DAC code written into the DACx register is clipped so that the code used to set the DAC voltage is actually given by

DACCode
= DACx, DNLIMx ≤ DACx ≤ DPLIMx
= DNLIMx, DACx < DPLIMx
= DPLIMx, DACx > DPLIMx

The DAC output buffer is three-stated if DNLIMx > DPLIMx. It is possible for the user to make it difficult for the DAC output buffers to be turned on at all in normal system operation by programming the limit registers in this way (these are among the registers downloaded from EEPROM at startup).

Table 18 shows the detail of the registers required to set up the DACs.

Table 18. DAC Configuration Registers

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
DAC1	0x50	DACCTRL1	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC1.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC1.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x58	DAC1	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x60	DPLIM1	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC1 is set to a higher code, the DAC code limits to the contents of this register.
	0x68	DNLIM1	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC1 is set to a lower code, the DAC code limits to the contents of this register. Note: if DNLIM1 is set to be greater than DPLIM1, the DAC output is always disabled (this is a safety feature).
DAC2	0x51	DACCTRL2	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC2.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC2.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x59	DAC2	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x61	DPLIM2	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC2 is set to a higher code, the DAC code limits to the contents of this register.
	0x69	DNLIM2	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC2 is set to a lower code, the DAC code limits to the contents of this register. Note: if DNLIM2 is set to be greater than DPLIM2, the DAC output is always disabled (this is a safety feature).
DAC3	0x52	DACCTRL3	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC3.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC3.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x5A	DAC3	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x62	DPLIM3	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC3 is set to a code higher than this, the DAC code limits to the contents of this register.
	0x6A	DNLIM3	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC3 is set to a code lower than this, the DAC code limits to the contents of this register. Note: if DNLIM3 is set to be greater than DPLIM3, the DAC output is always disabled (this is a safety feature).

Output	Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
DAC4	0x53	DACCTRL4	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC4.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC4.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x5B	DAC4	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x63	DPLIM4	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC4 is set to a higher code, the DAC code limits to the contents of this register.
	0x6B	DNLIM4	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC4 is set to a lower code, the DAC code limits to the contents of this register. Note: if DNLIM4 is set to be greater than DPLIM4, the DAC output is always disabled (this is a safety feature).
DAC5	0x54	DACCTRL5	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC5.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC5.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x5C	DAC5	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F Is midcode).
	0x64	DPLIM5	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC5 is set to a higher code, the DAC code limits to the contents of this register.
	0x6C	DNLIM5	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC5 is set to a lower code, the DAC code limits to the contents of this register. Note: if DNLIM5 is set to be greater than DPLIM5, the DAC output is always disabled (this is a safety feature).
DAC6	0x55	DACCTRL6	7:3	N/A		Cannot be used.
			2	ENDAC	R/W	Enables DAC6.
			1:0	OFFSEL1 to OFFSEL0	R/W	Selects the center voltage (midcode) output of DAC5.
						OFFSEL1 / **OFFSEL0** / **(Midcode) Output Voltage**: 0 / 0 / 1.25 V; 0 / 1 / 1.0 V; 1 / 0 / 0.8 V; 1 / 1 / 0.6 V
	0x5D	DAC6	7:0	DAC7 to DAC0	R/W	8-bit DAC code (0x7F is midcode).
	0x65	DPLIM6	7:0	LIM7 to LIM0	R/W	8-bit DAC positive limit code. If DAC6 is set to a higher code, the DAC code limits to the contents of this register.
	0x6D	DNLIM6	7:0	LIM7 to LIM0	R/W	8-bit DAC negative limit code. If DAC6 is set to a lower code, the DAC code limits to the contents of this register. Note: if DNLIM6 is set to be greater than DPLIM6, the DAC output is always disabled (this is a safety feature).

WARNINGS, FAULTS, AND STATUS

WARNINGS

The ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 devices feature a lower level of fault detection that can be used in conjunction with the fault detection provided on the inputs. These lower level fault reports are provided by the ADC limit registers and by the secondary SFDs on the VP1 to VP4 and VH inputs. (The secondary SFDs are available on these pins when VX1 to VX5 are used as digital inputs; see the Inputs section.)

WARNING is provided as a single input to the SE. It consists of a wide OR of the ADC limit registers and the secondary SFD outputs. Selecting WARNING as an input to the SE is shown in the Sequencing Engine section.

FAULT/STATUS REPORTING

If a fault occurs on one of the inputs being monitored by the ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 (that is, a supply on one of the VXx/VPx/VH pins moves outside its threshold window), a logic level is deasserted, or an ADC input violates the limit set in its limit register, it is possible to identify exactly on which input the fault occurred. This is done by reading back the fault plane over the SMBus.

The fault plane is simply two registers, FSTAT1 and FSTAT2, where each bit represents a function, for example, a VPx pin or an ADC channel. By reading the contents of these registers and determining which bits are set to 1, the user can identify the inputs on which faults have occurred. A 1 is defined as a fault. The exception to this is when a VXx pin is used as a digital input. In that case, 1 is the true logic value of the input on the pin.

The fault data is reported to the fault plane only if explicitly enabled. This is done by setting the fault latch bit high in each individual state. To do this, set Bit 63 in the relevant state configuration to 1 (see Table 5). If this bit is not set, a fault that occurs in this state is not latched in the fault plane. The ADM1062/ADM1063/ADM1064/ADM1065/ADM1066/ADM1067/ADM1166 also feature a number of status registers that can be read at any time to determine the status of the inputs. The contents of these registers can change at any time; that is, the data is not latched in these registers as is the case with FSTAT1 and FSTAT2. Table 19 shows the details of the fault and status registers.

Table 19. Fault and Status Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xE0	FSTAT1	7	FLT_VX3	R	Fault output from the VX3 pin (either as a GPI or as an SFD).
		6	FLT_VX2	R	Fault output from the VX2 pin (either as a GPI or as an SFD).
		5	FLT_VX1	R	Fault output from the VX1 pin (either as a GPI or as an SFD).
		4	FLT_VH	R	Fault output from the VH SFD.
		3	FLT_VP4	R	Fault output from the VP4 SFD.
		2	FLT_VP3		Fault output from the VP3 SFD.
		1	FLT_VP2		Fault output from the VP2 SFD.
		0	FLT_VP1		Fault output from the VP1 SFD.
0xE1	FSTAT2	7:2			Cannot be used.
		1	FLT_VX5	R	Fault output from the VX5 pin (either as a GPI or as an SFD).
		0	FLT_VX4	R	Fault output from the VX4 pin (either as a GPI or as an SFD).
0xE2	OVSTAT1	7	OV_VX3	R	OV threshold exceeded on VX3 (SFD) or VP3 (warning).
		6	OV_VX2	R	OV threshold exceeded on VX2 (SFD) or VP2 (warning).
		5	OV_VX1	R	OV threshold exceeded on VX1 (SFD) or VP1 (warning).
		4	OV_VH	R	OV threshold exceeded on the VH SFD.
		3	OV_VP4	R	OV threshold exceeded on the VP4 SFD.
		2	OV_VP3	R	OV threshold exceeded on the VP3 SFD.
		1	OV_VP2	R	OV threshold exceeded on the VP2 SFD.
		0	OV_VP1	R	OV threshold exceeded on the VP1 SFD.
0xE3	OVSTAT2	7:2			Cannot be used.
		1	OV_VX5	R	OV threshold exceeded on VX5 (SFD) or VH (warning).
		0	OV_VX4	R	OV threshold exceeded on VX4 (SFD) or VP4 (warning).
0xE4	UVSTAT1	7	UV_VX3	R	UV threshold exceeded on VX3 (SFD) or VP3 (warning).
		6	UV_VX2	R	UV threshold exceeded on VX2 (SFD) or VP2 (warning).
		5	UV_VX1	R	UV threshold exceeded on VX1 (SFD) or VP1 (warning).
		4	UV_VH	R	UV threshold exceeded on the VH SFD.
		3	UV_VP4	R	UV threshold exceeded on the VP4 SFD.
		2	UV_VP3	R	UV threshold exceeded on the VP3 SFD.

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
		1	UV_VP2	R	UV threshold exceeded on the VP2 SFD.
		0	UV_VP1	R	UV threshold exceeded on the VP1 SFD.
0xE5	UVSTAT2	7:2			Cannot be used.
		1	UV_VX5	R	UV threshold exceeded on VX5 (SFD) or VH (warning).
		0	UV_VX4	R	UV threshold exceeded on VX4 (SFD) or VP4 (warning).
0xE6	LIMSTAT1	7	VX3 CH	R	VX3 limit status – used with LSENSE 1.
		6	VX2 CH	R	VX2 limit status – used with LSENSE 1.
		5	VX1 CH	R	VX1 limit status – used with LSENSE 1.
		4	VH CH	R	VH limit status – used with LSENSE 1.
		3	VP4 CH	R	VP4 limit status – used with LSENSE 1.
		2	VP3 CH	R	VP3 limit status – used with LSENSE 1.
		1	VP2 CH	R	VP2 limit status – used with LSENSE 1.
		0	VP1 CH	R	VP1 limit status – used with LSENSE 1.
0xE7	LIMSTAT2	4	EXTS2	R	EXTS2 limit status – used with LSENSE 2. ADM1063 only.
		3	AUX2	R	AUX2 limit status – used with LSENSE 2. ADM1064 and ADM1066 only.
		3	EXTS1	R	EXTS1 limit status – used with LSENSE 2. ADM1062 and ADM1063 only.
		2	AUX1	R	AUX1 limit status – used with LSENSE 2. ADM1064 and ADM1066 only.
		2	IN TS	R	IN TS limit status – used with LSENSE 2. ADM1062 and ADM1063 only.
		1	VX5 CH	R	VX5 CH limit status – used with LSENSE 2.
		0	VX4 CH	R	VX4 CH limit status – used with LSENSE 2.
0xE8	GPISTAT	7:5			Cannot be used.
		4	VX5_STAT	R	VX5 GPI input status (after signal conditioning).
		3	VX4_STAT	R	VX4 GPI input status (after signal conditioning).
		2	VX3_STAT	R	VX3 GPI input status (after signal conditioning).
		1	VX2_STAT	R	VX2 GPI input status (after signal conditioning).
		0	VX1_STAT	R	VX1 GPI input status (after signal conditioning).

BLACK BOX STATUS REGISTERS AND FAULT RECORDS ON THE ADM1166

Each time the ADM1166 sequence engine changes state, the contents of UVSTATx, OVSTATx, LIMSTATx, and GPISTATx, along with some other pieces of information relating to the sequence engine state and the cause of the last state transition, are latched into seven black box status registers.

These registers provide a snapshot of the state of the inputs being monitored by the ADM1166, what the last state was, and what caused the last state change.

After the sequence engine changes state, if the new state it enters has its corresponding BBWRTRGx.STATEy bit set, the seven black box status registers are written sequentially into the next available location in the black box EEPROM section.

After the seven bytes are written, an eighth checksum byte is written to provide a method to check data integrity. This can be important if only a partial record is written because all the supplies powering the part have failed.

The order of the bytes in a fault record stored in EEPROM is as follows:

- PREVSTEXT
- PREVSEQST
- BBSTAT1
- BBSTAT2
- BBSTAT3
- BBSTAT4
- BBSTAT5
- CHECKSUM

The bytes are stored from lowest EEPROM address to highest; therefore, for the first fault record location in the black box EEPROM, PREVSTEXT would be stored at 0xF980 and CHECKSUM at 0xF987.

USE OF THE REVID REGISTER

The ADM1066 and ADM1166 have the same I²C addresses range, and both return the value of 0x41 when the MANID register is read. REVID is a read-only register that can be used to determine whether a device at a given address is an ADM1066 or an ADM1166. This is detailed in Table 21.

Table 20. ADM1166 Black Box Fault and Status Registers

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xEA	PREVSTEXT	7	BBUSED		Always reads as 0. When this bit is written to the first byte of a fault record in EEPROM, it marks all eight bytes in use. When the black box is searching for the next free location to use, this bit is examined. If this bit is 0, then even if the previous fault record was only partially written to EEPROM, the eight bytes of the fault record are ignored.
		6	Reserved		Always reads as 0.
		5	SMBJUMP	R	Indicates that the previous state transition was due to an SMBJump being received.
		4	LIMWARN	R	Indicates that the previous state transition was due to one or more ADC warning limits being exceeded.
		3	SFDCMP	R	Indicates that the previous state transition was due to one or more supply fault detector limits being exceeded.
		2	Timeout	R	Indicates that the previous state transition was due to the timeout condition becoming true.
		1	Monitor	R	Indicates that the previous state transition was due to the monitor condition becoming true.
		0	Sequence	R	Indicates that the previous state transition was due to the sequence condition becoming true.
0xEB	PREVSEQST	7:6			Cannot be used.
		5:0	PREVADDR	R	State number of the state that was active immediately prior to the current state.
0xEC	BBSTAT 1	7	UV_VX3	R	UV threshold exceeded on VX3 (SFD) or VP3 (warning).
		6	UV_VX2	R	UV threshold exceeded on VX2 (SFD) or VP2 (warning).
		5	UV_VX1	R	UV threshold exceeded on VX1 (SFD) or VP1 (warning).
		4	UV_VH	R	UV threshold exceeded on the VH SFD.
		3	UV_VP4	R	UV threshold exceeded on the VP4 SFD.
		2	UV_VP3	R	UV threshold exceeded on the VP3 SFD.
		1	UV_VP2	R	UV threshold exceeded on the VP2 SFD.
		0	UV_VP1	R	UV threshold exceeded on the VP1 SFD.
0xED	BBSTAT2	7	OV_VX1	R	OV threshold exceeded on VX1 (SFD) or VP1 (warning).
		6	OV_VH	R	OV threshold exceeded on the VH SFD.
		5	OV_VP4	R	OV threshold exceeded on the VP4 SFD.
		4	OV_VP3	R	OV threshold exceeded on the VP3 SFD.
		3	OV_VP2	R	OV threshold exceeded on the VP2 SFD.
		2	OV_VP1	R	OV threshold exceeded on the VP1 SFD.
		1	UV_VX5	R	UV threshold exceeded on VX5 (SFD) or VH (warning).
		0	UV_VX4	R	UV threshold exceeded on VX4 (SFD) or VP4 (warning).
0xEE	BBSTAT3	7	VX4_STAT	R	VX4 GPI input status (after signal conditioning).
		6	VX3_STAT	R	VX3 GPI input status (after signal conditioning).
		5	VX2_STAT	R	VX2 GPI input status (after signal conditioning).
		4	VX1_STAT	R	VX1 GPI input status (after signal conditioning).
		3	OV_VX5	R	OV threshold exceeded on VX5 (SFD) or VH (warning).
		2	OV_VX4	R	OV threshold exceeded on VX4 (SFD) or VP4 (warning).
		1	OV_VX3	R	OV threshold exceeded on VX3 (SFD) or VP3 (warning).
		0	OV_VX2	R	OV threshold exceeded on VX2 (SFD) or VP2 (warning).
0xEF	BBSTAT4	7	VX2 CH	R	VX2 limit status – used with LSENSE 1.
		6	VX1 CH	R	VX1 limit status – used with LSENSE 1.
		5	VH CH	R	VH limit status – used with LSENSE 1.
		4	VP4 CH	R	VP4 limit status – used with LSENSE 1.
		3	VP3 CH	R	VP3 limit status – used with LSENSE 1.
		2	VP2 CH	R	VP2 limit status – used with LSENSE 1.
		1	VP1 CH	R	VP1 limit status – used with LSENSE 1.
		0	VX5_STAT	R	VX5 GPI input status (after signal conditioning).

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0x F0	BBSTAT5	7:5			Cannot be used.
		4	AUX2	R	AUX2 limit status – used with LSENSE 2. ADM1064 and ADM1066 only.
		3	AUX1	R	AUX1 limit status – used with LSENSE 2. ADM1064 and ADM1066 only.
		2	VX5 CH	R	VX5 CH limit status – used with LSENSE 2.
		1	VX4 CH	R	VX4 CH limit status – used with LSENSE 2.
		0	VX3 CH	R	VX3 limit status – used with LSENSE 1.
0x F1	BBADDR	7:0	ADDR	R	Low byte of the address location in the 0xF980 to 0xF9FF range that the next fault record is written to. When no fault records have been written, the value is 0x80, and increments by 8 each time a fault record is written. The value is 0x F8 when there is only one fault record not written. When all locations have been written to, and the black box EEPROM is full, the value is 0x00.

Table 21. Decoding the REVID Register.

Reg.	Reg. Name	Bits	Mnemonic	R/W	Description
0xF5	REVID	7:4	Family	R	When the value 0x0 is read, the device is an ADM1062/ADM1063/ADM1064/ ADM1065/ADM1066/ADM1067. When the value 0x1 is read, the device is an ADM1166.
		3:0	HWVER	R	This value is the hardware revision number.

Table 22. Register Map Quick Reference[1]

Base (Hex)	Function	0	1	2	3	4	5	6	7
00	VP1	PS1OVTH	PS1OVHYST	PS1UVTH	PS1UVHYST	SFDV1CFG	SFDV1SEL	x	PDO1CFG
08	VP2	PS2OVTH	PS2OVHYST	PS2UVTH	PS2UVHYST	SFDV2CFG	SFDV2SEL	x	PDO2CFG
10	VP3	PS3OVTH	PS3OVHYST	PS3UVTH	PS3UVHYST	SFDV3CFG	SFDV3SEL	x	PDO3CFG
18	VP4	PS4OVTH	PS4OVHYST	PS4UVTH	PS4UVHYST	SFDV4CFG	SFDV4SEL	x	PDO4CFG
20	VH	PSVHOVTH	PSVHOVHYST	PSVHUVTH	PSVHUVHYST	PSVHDVHCFG	SFDVHSEL	x	PDO5CFG
28	VX1	X1OVTH	X1OVHYST	X1UVTH	X1UVHYST	SFDX1CFG	SFDX1SEL	XGPI1CFG	PDO6CFG
30	VX2	X2OVTH	X2OVHYST	X2UVTH	X2UVHYST	SFDX2CFG	SFDX2SEL	XGPI2CFG	PDO7CFG
38	VX3	X3OVTH	X3OVHYST	X3UVTH	X3UVHYST	SFDX3CFG	SFDX3SEL	XGPI3CFG	PDO8CFG
40	VX4	X4OVTH	X4OVHYST	X4UVTH	X4UVHYST	SFDX4CFG	SFDX4SEL	XGPI4CFG	PDO9CFG
48	VX5	X5OVTH	X5OVHYST	X5UVTH	X5UVHYST	SFDX5CFG	SFDX5SEL	XGPI5CFG	PDO10CFG
50	DAC control	DACCTRL1	DACCTRL2	DACCTRL3	DACCTRL4	DACCTRL5	DACCTRL6	x	x
58	DAC code	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6	x	x
60	DAC upper limit	DPLIM1	DPLIM2	DPLIM3	DPLIM4	DPLIM5	DPLIM6	x	x
68	DAC lower limit	DNLIM1	DNLIM2	DNLIM3	DNLIM4	DNLIM5	DNLIM6	x	x
70	ADCLIM	ADCVP1LIM	ADCVP2LIM	ADCVP3LIM	ADCVP4LIM	ADCVHLIM	ADCVX1LIM	ADCVX2LIM	ADCVX3LIM
78	ADCLIM	ADCVX4LIM	ADCVX5LIM	ADCITLIM	ADCXTS1LIM	ADCXTS2LIM	LSENSE1	LSENSE2	x
80	ADC setup	RRSEL1	RRSEL2	RRCTRL	TSCTRL	x	x	x	x
88		x	x	x	x	x	x	x	x
90	Miscellaneous	UPDCFG	PDEN1	PDEN2	SECTRL	BBWRTRG1[2]	BBWRTRG2[2]	BBWRTRG3[2]	BBWRTRG4[2]
98	Miscellaneous	BBWRTRG5[2]	BBWRTRG6[2]	BBWRTRG7[2]	BBWRTRG8[2]	BBCTRL[2]	x	x	x
A0	ADC readback	ADCHVP1	ADCLVP1	ADCHVP2	ADCLVP2	ADCHVP3	ADCLVP3	ADCHVP4	ADCLVP4
A8	ADC readback	ADCHVH	ADCLVH	ADCHVX1	ADCLVX1	ADCHVX2	ADCLVX2	ADCHVX3	ADCLVX3
B0	ADC readback	ADCHVX4	ADCLVX4	ADCHVX5	ADCLVX5	ADCHITS	ADCLITS	ADCHXTS1	ADCLXTS1
B8	ADC readback	ADCHXTS2	ADCLXTS2	x	x	x	x	x	x
C0		x	x	x	x	x	x	x	x
C8		x	x	x	x	x	x	x	x
D0		x	x	x	x	x	x	x	x
D8	Miscellaneous	UDOWNLD	BBSEARCH[2]	UNLOCKSE[2]	SEDOWNLD[2]	x	x	x	x
E0	Fault (read-only)	FSTAT1	FSTAT2	OVSTAT1	OVSTAT2	UVSTAT1	UVSTAT2	LIMSTAT1	LIMSTAT2
E8	Fault (read-only)	GPISTAT	SEADDR	PREVSTEXT[2]	PREVSEQST[2]	BBSTAT1[2]	BBSTAT2[2]	BBSTAT4[2]	BBSTAT4[2]
F0	Miscellaneous	BBSTAT5[2]	BBADDR[2]	x	x	MANID	REVID	MARK1	MARK2
F8	Commands	EEALOW	EEAHIGH	EEBLOW	EEBHIGH	BLKWR	BLKRD	BLKER	x

[1] x indicates that register locations do not exist.
[2] Available only on the ADM1166.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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