AN-1420
APPLICATION NOTE

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Phase Buildout and Hitless Switchover with Digital Phase-Locked Loops (DPLLs)

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INTRODUCTION

Analog Devices, Inc., incorporates DPLL technology in an array of clock and timing products. Besides frequency translation flexibility, the DPLL technology offers a host of system enabling digital functionalities, such as clock validation, phase or frequency controllable switching, and accurate and smooth transition into and out of holdover. This application note discusses the reference switchover operation and its capabilities.

TYPES OF SWITCHOVER

There are two types of switchover: phase buildout and hitless. Because there is no universal definition of the two types, they are defined in this application note as follows:

- Phase buildout is the phase difference between the two references when the switching time is built out into the DPLL. This phase difference is the phase offset between the output and the active reference in lock.
- Hitless is similar to zero delay, where the output phase tracks the active reference phase after phase lock is acquired.

For more information about hitless and phase buildout switchover operation from Reference A to Reference B, consider the examples described in the Same Frequency Switching section and the Different Frequencies Switching section.

SAME FREQUENCY SWITCHING

In Figure 1 and Figure 2, Reference A and Reference B have the same frequency and phase offset, ΔΦ.

Phase Buildout Mode—Same Frequency

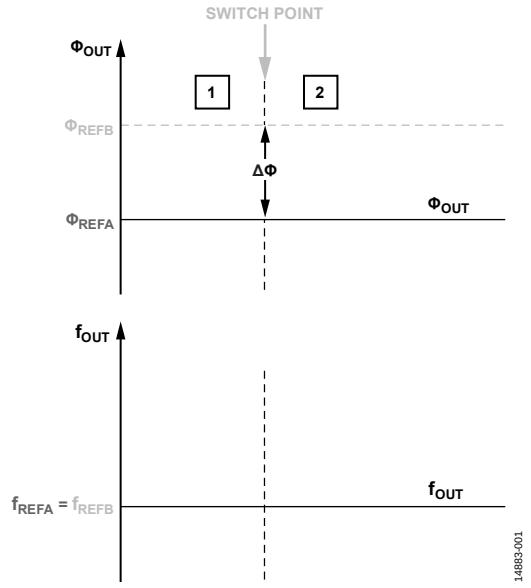

Figure 1. Phase Buildout Mode with Reference A and Reference B Having the Same Frequency

Region 1

Reference A is active. The DPLL locks to Reference A, in both phase and frequency. Assume that there is no phase offset, $\Phi_{OUT} = \Phi_{REFA}$, and $f_{OUT} = f_{REFA}$. Φ_{OUT} is the output phase, and f_{OUT} is the output frequency.

Switch Point

Reference B becomes active. The phase offset, ΔΦ, between Reference A and Reference B is built out into the phase frequency detector (PFD) of the DPLL as an offset.

Region 2

The DPLL then locks to Reference B, with $\Phi_{OUT} = \Phi_{REFA}$ and $f_{OUT} = f_{REFA} = f_{REFB}$. There is a fixed phase offset of ΔΦ between the output and the active Reference B. Fixed phase offset is a typical characteristic of a phase buildout.

Hitless Mode—Same Frequency

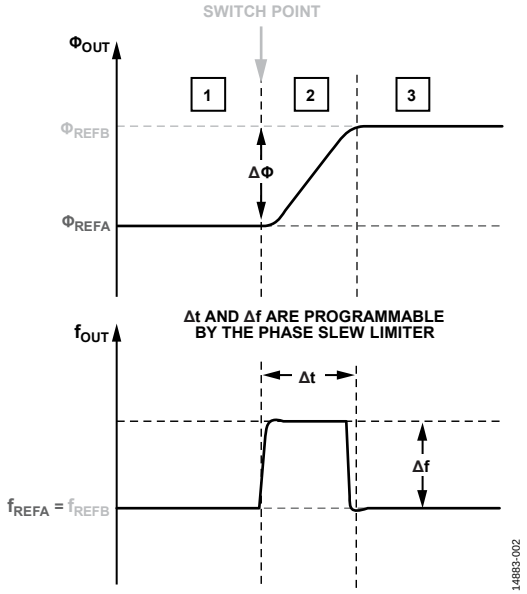

Figure 2. Hitless Mode with Reference A and Reference B Having the Same Frequency

Region 1

Reference A is active. The DPLL locks to Reference A, in both phase and frequency. Assume that there is no phase offset, $\Phi_{OUT} = \Phi_{REFA}$ and $f_{OUT} = f_{REFA}$.

Switch Point

Reference B becomes active. The phase difference of the references is ΔΦ.

Region 2

The DPLL slews the output phase from Φ_{REFA} to Φ_{REFB}. During this lock time (Δt) transition period, there is a frequency excursion of Δf, which is inversely proportional to Δt, that is, the shorter the lock time, the larger the frequency excursion. For Analog Devices DPLL clock products, control the lock time and frequency excursion by setting the phase slew rate.

Region 3

The DPLL then locks to Reference B, with $\Phi_{OUT} = \Phi_{REFA}$ and $f_{OUT} = f_{REFB}$. For hitless switching, there is no phase offset between the output and the active reference.

DIFFERENT FREQUENCIES SWITCHING

In Figure 3 and Figure 4, Reference A and Reference B have different frequencies.

Phase Buildout Mode—Different Frequencies

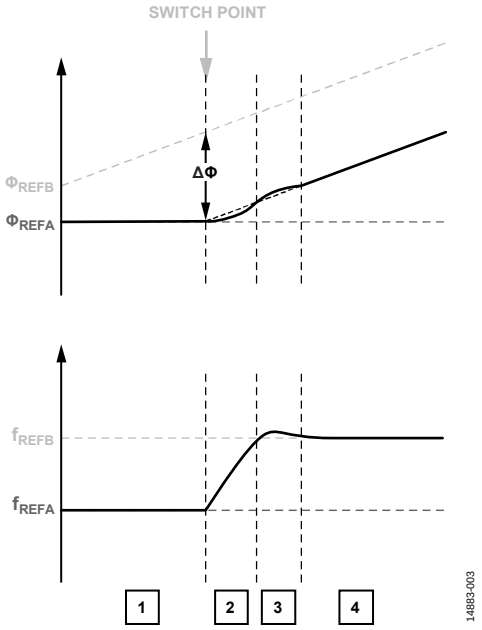

Figure 3. Phase Buildout Mode with Reference A and Reference B Having Different Frequencies

Region 1

Reference A is active. The DPLL locks to Reference A, in both phase and frequency. Assume that there is no phase offset, $\Phi_{OUT} = \Phi_{REFA}$ and $f_{OUT} = f_{REFA}$.

Switch Point

Reference B becomes active. The phase difference of the references is ΔΦ at this switch point.

Region 2

The DPLL attempts to acquire frequency lock. At the switching point, the phase difference between the references, ΔΦ, is built out into the PFD of the DPLL. The system is unlocked in both phase and frequency during this period.

Region 3

The DPLL is frequency locked to Reference B and is acquiring phase lock to Reference B with the buildout phase offset of ΔΦ. In both Region 2 and Region 3, the locking time and frequency excursion are automanaged. The phase slew limiter has no effect on Δt and Δf in this case.

Region 4

The DPLL is both phase and frequency locked to Reference B, with $\Phi_{OUT} = \Phi_{REFB} - \Delta\Phi$ and $f_{OUT} = f_{REFB}$. There is a fixed phase offset of ΔΦ between the output and its active Reference B, indicative of phase buildout mode.

Hitless Mode—Different Frequencies

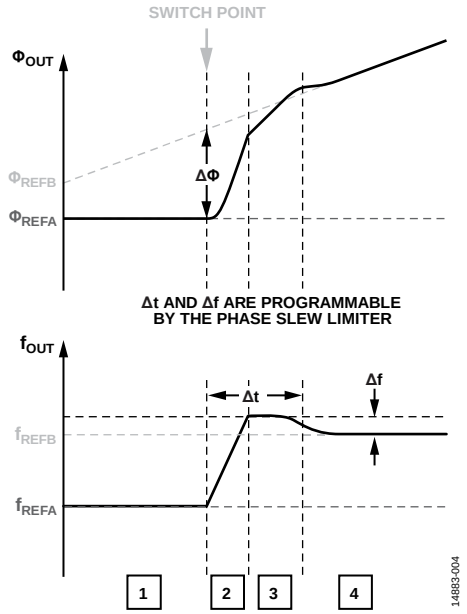

Figure 4. Hitless Mode with Reference A and Reference B Having Different Frequencies

Region 1

Reference A is active. The DPLL locks to Reference A, in both phase and frequency. Assume that there is no phase offset, $\Phi_{OUT} = \Phi_{REFA}$ and $f_{OUT} = f_{REFA}$.

Switch Point

Reference B becomes active. The phase offset between the references is $\Delta\Phi$.

Region 2

The DPLL attempts to acquire frequency lock. The system is unlocked in both phase and frequency during this period. The phase slew limiter is active during this period, allowing management of lock time and frequency excursion.

Region 3

The DPLL is frequency locked to Reference B, and is acquiring phase lock to Reference B. The phase slew limiter is also active during this period, allowing management of lock time and frequency excursion.

Region 4

The DPLL is both phase and frequency locked to Reference B, with $\Phi_{OUT} = \Phi_{REFB}$ and $f_{OUT} = f_{REFB}$.